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# Development of Low Temperature Oxidation Process Using Ozone For VlSI

**Yudhvir Singh Chib**

Electronics & Communication Department, Thapar University, Patiala, India

**Abstract**: With decreasing size of MOS transistor the thickness of gate oxide ($SiO_2$) is reaching in regime where it is just 2-3 atomic layers thick about 1 to 1.5 nm thick because of thin oxide layers there is direct tunnelling of charge carriers through gate oxide, and the transport of charge carriers through defects in gate oxide. The increasing leakage current through gate oxide is proving to be a showstopper to the scaling of MOS transistor, and saturating the Moore's Law. For the applications, where the devices are need to be fabricated on plastic, glass or poly-crystalline silicon substrates a good quality of oxide is required to be grown at low temperatures. In this work a low temperature, defect free oxide growth technique using ozone is presented and we study the effect of various ambient temperatures on growth of $SiO_2$, the effect of pre cleaning and passivation on quality of ozone grown oxide in terms of bulk defect density, Si-$SiO_2$ interface trap charge density and on oxide life time is presented.

**Keywords**: MOS (Metal Oxide Semiconductor), FET (Field Effect Transistor), TDDB (Time Dependent Dielectric Breakdown), $D_{it}$ (Density of Interface Traps).

## I. INTRODUCTION

The oxidation process of silicon is the heart of all the fabrication steps followed in fabricating a MOSFET and makes a MOFET functional. But with the advancement in the IC technology and diminishing size of MOSFET's this crucial $SiO_2$ is getting thinner and thinner. The thickness of $SiO_2$ currently required is less than 1 nm [1], which is just 3 monolayer of $SiO_2$ (1 monolayer ~ 0.3nm). For the performance evaluation MOSFETs, the most basic factor is the current between source and drain, which the transistor is able to drive. More current shows that the transistor can be operated faster and all the parasitic capacitances and resistances within that transistor are having a lesser impact on MOSFET. Firstly, the gate voltage, applied between gate electrode and substrate separated by a dielectric material to form a parallel plate capacitor type arrangement, and the accumulation or inversion of the charge carriers is induced in the substrate on its application. The higher performance demanded from the transistor. From the basics of the MOSFET operation; we know there are two voltages available to control the operation of the value of capacitance signifies more inversion charge carriers in the semiconductor channel for the same applied voltage. And the second one is the voltage, which we apply between source, and drain, which is accountable for driving the induced charges forward in the channel. Thus $SiO_2$ is the dielectric material, which made FET transistors to work in silicon technology.

Significant properties of $SiO_2$ are as follows:

a) The high quality interface between Si and $SiO_2$.
b) Chemical and thermal stability at high temperature
c) (~$1000^0$C).
d) Good quality of insulation.
e) d)The hard mask in different diffusion and doping process.
f) High breakdown fields of 13 MV/cm.

Conventionally, molecular oxygen is used to grow the $SiO_2$ layer. In this process the silicon wafer is subjected to high temperature (900 °C – 1200 °C), which in turn exerts a lot of thermal stress on the wafer, alters doping profile and causes the elevated thermal budget. However, this high temperature in conventional process of oxidation cannot be applied to the modern substrates such as plastics and glass. Thus, there is the need of development of a new oxidation method. which is feasible at lower temperature and thus the thermal stress on the wafer can be reduced as well as reducing processing cost.

Use of ozone for oxidation of silicon at comparatively much lower temperatures is an attractive option. Ozone is a tri-atomic allotrope of oxygen, with symmetrical bent structure with an angle of $116^049$', and equal oxygen-oxygen bond length of 0.128 nm [2]. Since, this O-O bond length is shorter than that in $H_2O_2$ and $O_2$ and hence it is characterized as a double bond with bond order of 1.7 [2]. Due to the high reactivity of ozone [2] it is a proposed oxidant [3] to grow high quality $SiO_2$ film at low temperatures, and thus overcoming issues associated with thermal oxidation.

## II. EXPERIMENT AND RESULTS

The performed experimental results are classified into following categories:

*A. Effect of pre cleaning and passivation on oxide quality.*

To study the effect of pre cleaning and passivation on oxide and oxide interface some samples are processed with certain fabrication steps and obtained MOS capacitors of five different device areas on two differently processed silicon substrate. The results obtained are shown in Table I.

One substrate is passivated with hydrogen (-H) and other one is with hydroxyl (-OH) and the effect observed in different optical and electrical characteristics are as follows:

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*Effect on optical thickness*: The optical thicknesses of both the samples are measured using spectroscopic reflectometry using the Nanocalc - DUV system from Ocean Optics Inc. Germany. The measurements are done at different locations on the sample and the results obtained are shown in Table II

*Effect on bulk defects*: Gate current through oxide of thickness in this range is mainly depended on two phenomenon 1) Tunnelling current 2) Charge hopping through bulk defects in SiO2 [16].The leakage currents density obtained for the devices of different area distributed across the wafer are shown in Figs. 1-5.

Table I Metal dots of different areas deposited

| | |
|---|---|
| Area 1 | 7.78e-2 $Cm^2$ |
| Area 2 | 4.62e-3 $Cm^2$ |
| Area 3 | 1.86e-3 $Cm^2$ |
| Area 4 | 3.317e-4 $Cm^2$ |
| Area 5 | 5.178e-5 $Cm^2$ |

Table II Optical thickness obtained using spectroscopic reflectometry

| | Maximum Thickness Recorded | Minimum Thickness Recorded | Average Thickness Recorded |
|---|---|---|---|
| -OH Passivated | 1.35nm | 1.18nm | 1.21nm |
| -H Passivated | 1.89nm | 1.65nm | 1.80nm |

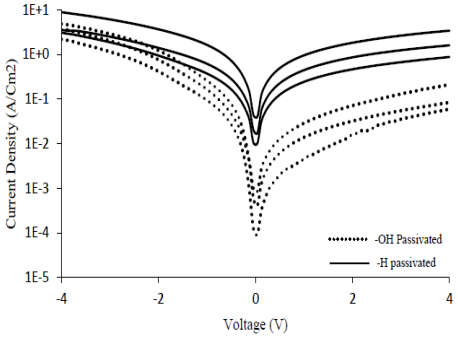


Fig. 1 Gate leakage current density for different devices of area 7.78e-3 $cm^2$ distributed across wafer.

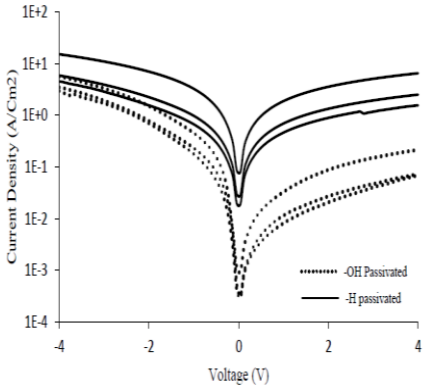


Fig. 2 Gate leakage current density for different devices of area 4.62e-3 $cm^2$ distributed across wafer.

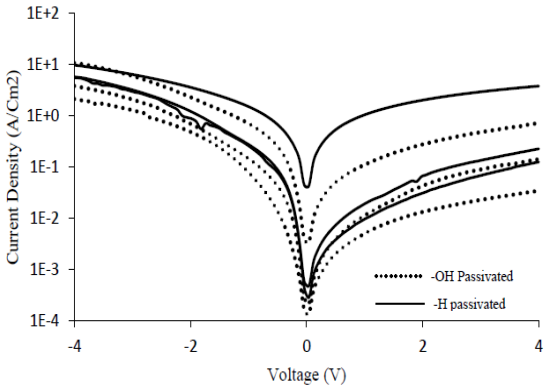


Fig. 3 Gate leakage current density for different devices of area 1.86e-3 $cm^2$ distributed across wafer.

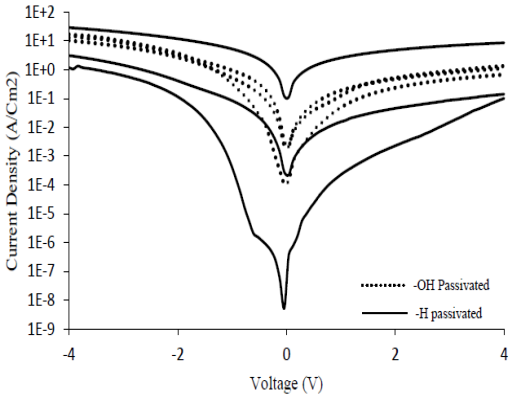


Fig. 4 Gate leakage current density for different devices of area 3.317e-4 $cm^2$ distributed across wafer.

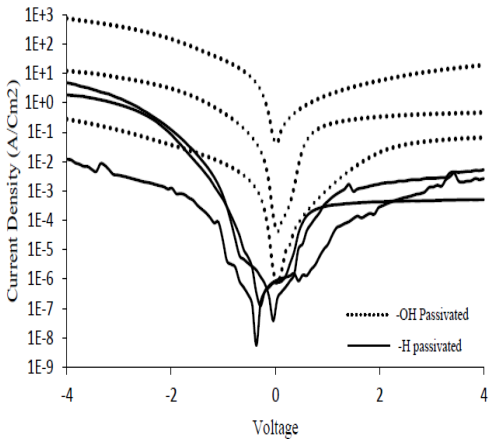


Fig. 5 Gate leakage current density for different devices of area 5.178e-5 $cm^2$ distributed across wafer.

We know that both –H and –OH covered silicon surface shows an initial repulsion to the $O_3$ molecule and thus initially cause a little inhibition in $SiO_2$ growth. But from the differences in the final optical thickness that we have measured, it can be concluded that –OH ions provide more inhibition for SiO2 growth. We have deduced the level of bulk defects present in both the oxides from J-V curves of devices of different dot areas for both type of passivation as the gate leakage is dependent on two factors 1) Tunneling of charge carriers 2) Conduction through bulk defects. The behaviors shown by leakage current density

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for small and large area devices shows that for large area devices the defect assisted leakage is prominent as compared to tunneling component of current in –H passivated devices even though the thickness is high as compared to –OH passivated but since defects are randomly distributed over area and thus the defect associated component is decreased with area and since tunneling is high in –OH passivated, for small areas the leakage current is high in –OH passivated.

*B. Effect on Si-SiO2 interface*

To get the effect of pre cleaning and passivation on Si-SiO2 C-V and Gp/ω vs f characterization of samples are been done and results are shown in Figs. 6-11.

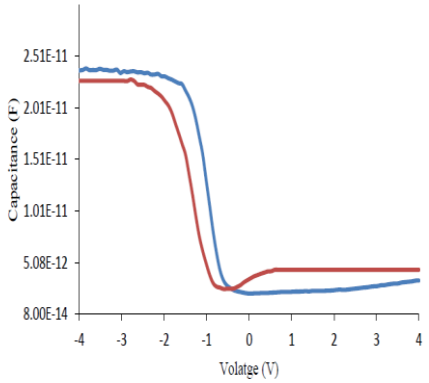


Fig. 6 CV characteristics of different MOS devices with –OH passivated Si, tox= 1.2 nm.

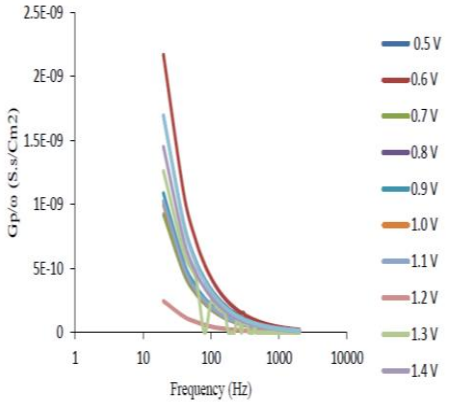


Fig. 7 Gp/ω Vs f characteristics MOS capacitor with –OH passivated Si at different gate voltages.

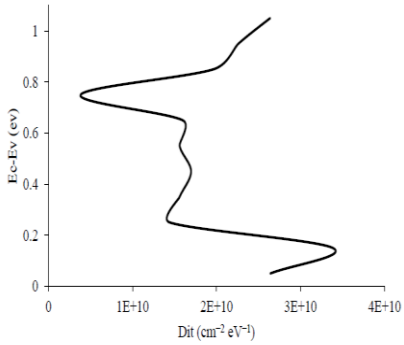


Fig. 8 Dit Vs position within Si band gap for –OH passivated Si.

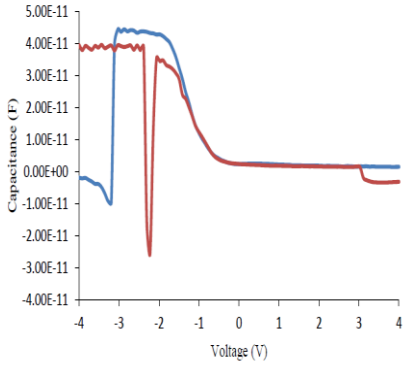


Fig. 9 CV characteristics of different MOS devices with –H passivated Si, tox= 2nm.

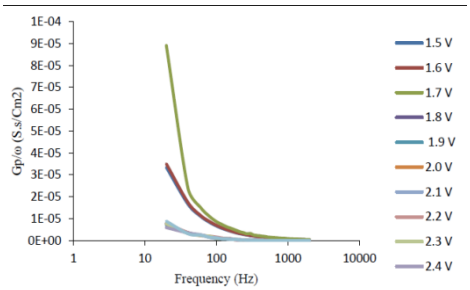


Fig. 10 Gp/ω Vs f characteristics MOS capacitor with –H passivated Si at different gate voltages.

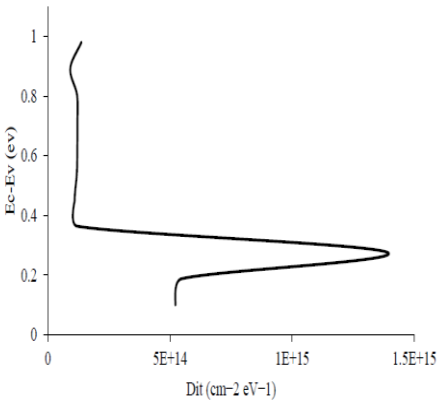


Fig. 11 Dit Vs position within Si band gap for –H passivated Si.

The density of interface trapped extracted for both –H and –OH passivated samples, make clear that there is huge difference in density of interface traps in both the samples. For –OH passivated samples the maximum Dit recorded is $3\times10^{10}$ while in –H passivated samples it is going to $1.5\times10^{15}$ which gives the difference five orders of difference. Even when we compare the ozone grown oxide with thermally grown oxide we can see three orders of improvement in density of interface traps shown in Fig. 12.

*C. Effect on oxide lifetime (TDDB)*

Time dependent dielectric breakdown analysis is a good method for life time estimation of $SiO_2$. This test is done at constant stress voltage to maintain the electric field of 6 MV/cm to 8 MV/cm and breakdown time is recorded. The results are shown in Figs. 13-17.

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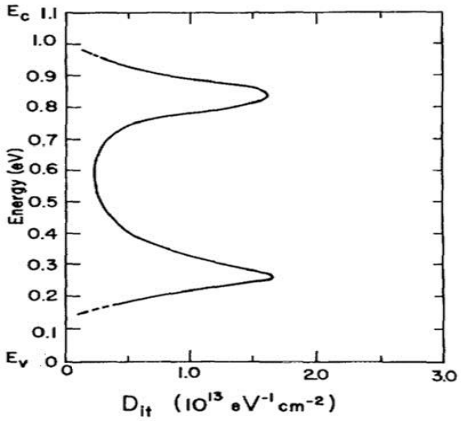


Fig 12 Density of interface traps in thermally grown oxide.

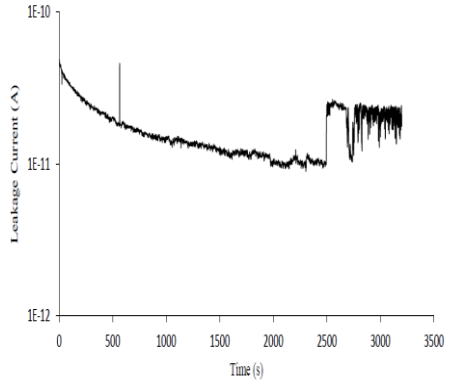


Fig. 13 Leakage current Vs Time for –OH passivated Si at stress voltage of 2 volts.

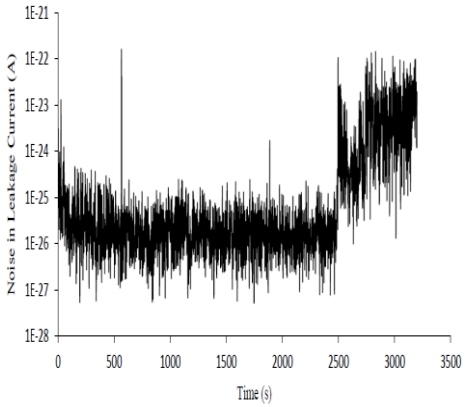


Fig. 14 Noise in leakage current Vs Time for –OH passivated Si at stress voltage of 2 volts

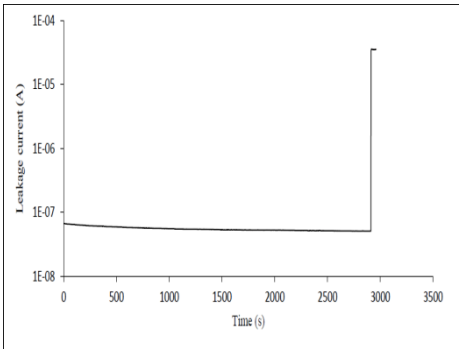


Fig. 15 Leakage current Vs Time for –OH passivated Si at stress voltage of 1.2 V.

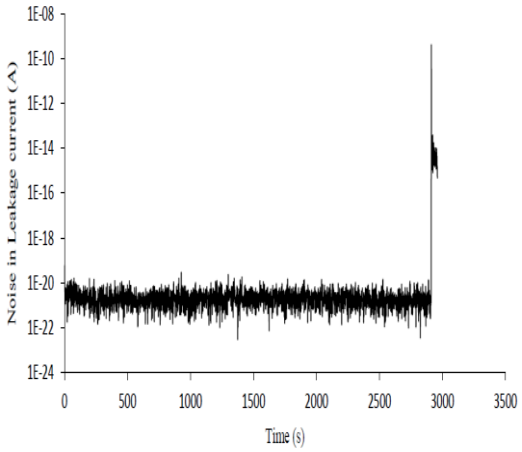


Fig. 16 Noise in leakage current Vs Time for –H passivated Si at stress voltage of 1.2 V.

From the TDDB experiment and measured in figure below we can conclude two important observations. Firstly, the most of the breakdown events occurred for –OH passivated silicon are soft while for –H passivated hard breakdown are more frequent and thus leads to catastrophic failure of devices. Secondly, even at high stress electric field for –OH passivated samples the breakdown is soft and time to breakdown is nearly equal to –H passivated samples those are stresses at lower electric field.

*D. Effect of oxidation temperature on oxide quality*

To study the effect of temperature on oxide quality MOS capacitor has been fabricated with oxide grown at different temperatures viz. 50°C, 100°C, 200°C, and 300°C with ozone flow rate of 0.5 liter/minute to obtain MOS capacitors. The results are shown in Figs. 18-25. The substrate is prepared by certain following the process steps. And this study is done on –OH passivated surface because –OH passivation is enhancing the oxide quality in every aspect as compared to –H passivated substrate. The diameter of metal electrode is 0.6 mm. C-V and I-V characterization is done for evaluation of parameter such as leakage current, oxide thickness and mobile trap charges. The C-V characterization is done at 100 Khz frequency at room temperature.

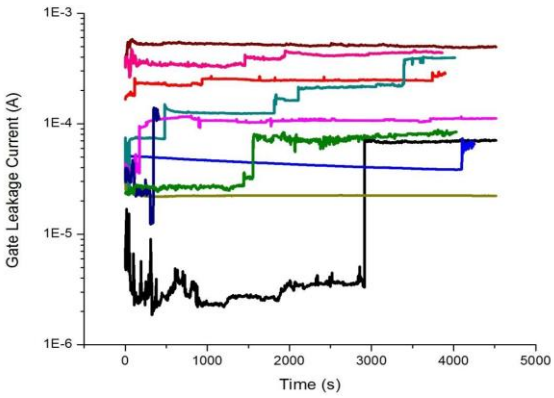


Fig. 17 TDDB in different devices of different areas at 2.8 stress voltage.

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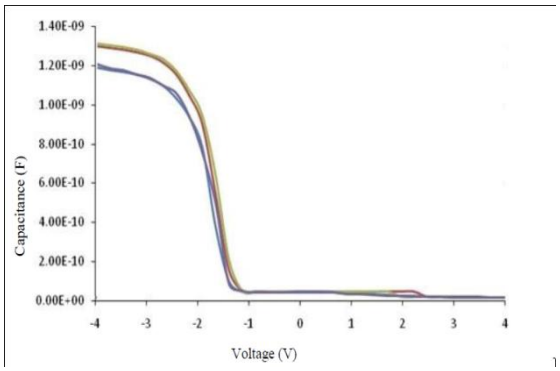


Fig. 18 CV characteristics of different devices at 50°C, tox= 2.5 – 3nm.

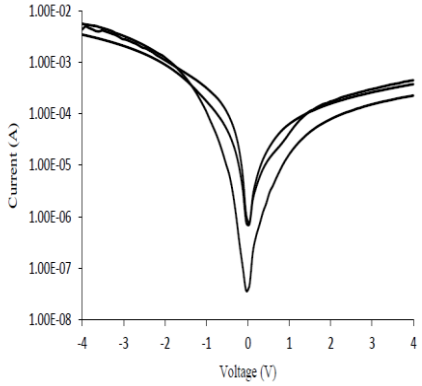


Fig. 19 IV characteristics of different devices at at 50°C.

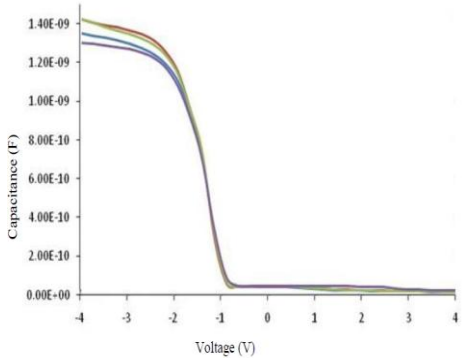


Fig. 20 CV characteristics of different devices at 100°C, tox= 2.5 – 3nm.

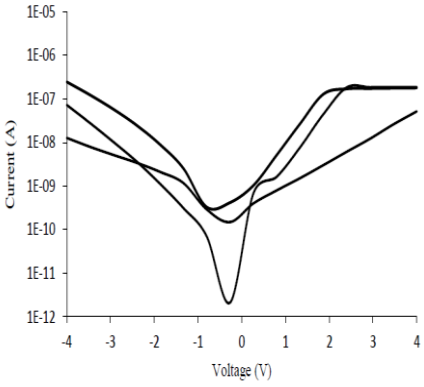


Fig. 21 IV characteristics of different devices at 100°C.

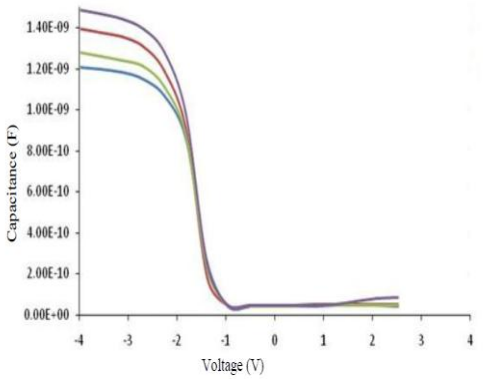


Fig. 22 CV characteristics of different devices at 200°C , tox= 2.5 – 3nm.

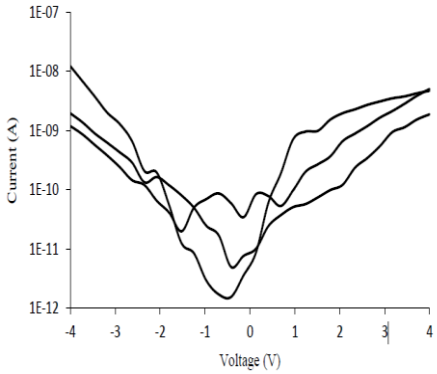


Fig. 23 IV characteristics of different devices at 200°C

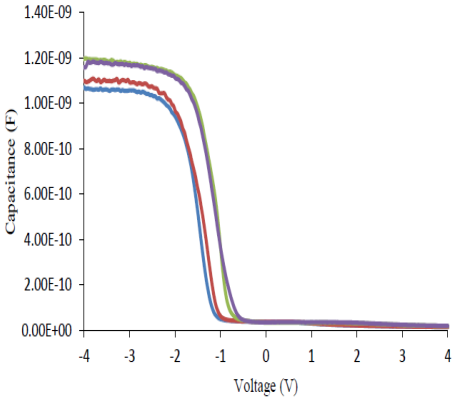


Fig. 24 CV characteristics of different devices at 300°C, tox= 2.5 – 3nm

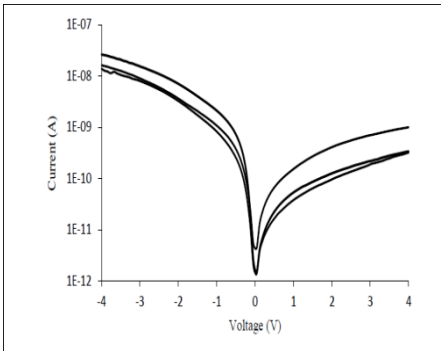


Fig. 25 IV characteristics of different devices at 300°C.

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*E. Effect of oxidation temperature on –OH passivated samples*

*Effect on oxide thickness:* The measured optical thickness as described above and the electrical thickness measured from accumulation capacitance in capacitance and voltage characteristics shows no significant change in the oxide thickness with change in temperature. For all the devices with oxide grown at different temperatures the oxide thickness recorded is between 2.5 nm – 3nm.

*Effect on oxide quality:* With increase in temperature, the drop in gate leakage current is observed even the thickness of SiO2 is nearly same which suggests that this increase in gate leakage current is due to increase in defect assisted leakage through SiO2 because for same oxide thickness the tunnelling current component are equal. And the increase in inversion to accumulation transition slope observed. Thus it is evident that with increase in oxidation temperature the quality of oxide is also enhancing.

Table III Maximum gate leakage current recorded for oxide grown at different temperatures.

| T °C | Maximum Current Recorded (A) | |
|---|---|---|
| | Accumulation Region | Inversion Region |
| 50 | $1\times10^{-2}$ | $1\times10^{-4}$ |
| 100 | $1\times10^{-6}$ | $1\times10^{-7}$ |
| 200 | $1\times10^{-8}$ | $1\times10^{-9}$ |
| 300 | $1\times10^{-8}$ | $1x10^{-10}$ |

## III. CONCLUSION

In this research we have done optical characterization, current voltage characterization, capacitance voltage characterization for estimation of oxide quality of –H passivated and –OH passivated samples. We have done Time dependent dielectric breakdown test for life time evaluation of both types of devices fabricated using different passivation technique. And lastly to study the effect of oxidation temperature on the quality of oxide on –OH passivated samples we have done I-V and C-V characterization of MOS devices with oxide grown at different temperatures. In this paper we have discussed various characterization techniques that we are going to use for evaluation of various parameters of SiO2, and using those parameters we can estimate the oxide quality in various growth conditions. For estimation of oxide bulk defects we have done I-V characterization and owing to its simple principle of bulk defects estimation, this experiment directly provides the estimation of bulk defect concentration without any sophisticated experiment.

For calculation of oxide thickness and flat band voltage we have straightforwardly used the capacitance voltage characterization thus from accumulation capacitance and from end of accumulation region in CV curves we will be able to calculate Tox and $V_{FB}$. But for the calculation of oxide life time we have to go through time taking constant voltage stress test. But for detection of breakdown in thin oxide we have done noise change detection. This method of ozone oxidation can be successfully applied to other semiconductor and High-κ materials for semiconductor applications. Many researchers have shown the application of ozone oxidation of SiGe, GaAs and SiC and many High-κ materials, which can be studied and similar kind of passivation techniques can be developed for improvement in oxide quality.

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