

Phase Locked Loop using VLSI Technology For Wireless Communication

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Abstract: Literature survey of Phase Locked Loop reflects that many researchers have applied different techniques like digital and analog simulation by applying mathematical/logical relations to design the Phase Locked Loop (PLL). Researchers have undertaken different systems, processes or phenomena with regard to design and attempted to find the unknown parameters and analysed PLL. Since in the real world today VLSI/CMOS is in very much in demand, it is observed that very few researchers have undertaken the work for designing PLL using CMOS/VLSI technology. The PLL is designed using 45 nm CMOS/VLSI technology in microwind 3.1. The main novelties related to the 45 nm technology are the high-k gate oxide, metal gate and very low-k interconnect dielectric. The effective gate length required for 45 nm technology is 25nm.

Keywords: Phase locked loop (PLL), voltage-controlled oscillator (VCO), 45nm technology, VLSI technology, low power

I. INTRODUCTION

A phase locked loop (PLL) is widely applied for different purposes in various domains such as communication and instrumentation. In the microwave range they have been applied in frequency synthesis and phase recovering among others. Phase-locked loop can be used to maintain a well-defined phase, and hence frequency relation between two independent signal sources. Due to their versatility, PLLs are usually preferred over other methods of maintaining phase lock such as injection locking. Monolithic phase locked loops have been used for clock-&-data recovery in communication system, clock generation & distribution in microprocessor and frequency synthesis in wireless application. Until DSP technology is capable of directly processing and generating the RF signals used to transmit wireless data, traditional RF engineering will remain a fundamental part of wireless communication systems design.

As it stands, wireless transceivers must still be able to generate a wide range of frequencies in order to up convert the outgoing data for transmission and down convert the received signal for processing. Monolithic phase locked loops have been used for clock-&-data recovery in communication system, clock generation and distribution in microprocessor and frequency synthesis in wireless application. The Phase locked loop is a feedback system as can be seen in the figure. It is a basic building block which is widely used in communications system such as mobile phones, which may contain up to 5 PLL's. Another important application are in motor speed control and for optical disk drive (ODD's) as found in DVD's and CD players. The basic PLL can be analog or digital. A phase locked loop (PLL) is used for different purposes in various sectors such as communication and instrumentation. In the

microwave range they are used in frequency synthesis and phase recovering among others. To maintain a well-defined phase and hence frequency relation between two independent signal sources, phase-locked loop can be used. Basic PLL consists of three elements: a phase detector, a loop filter and a voltage controlled oscillator (VCO) as shown in figure.

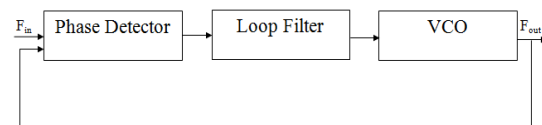


Figure 1.1: Block diagram of PLL

The output voltage of phase detector is proportional to the phase difference between the VCO's output signal and the reference. The phase detector's output produces a regular square oscillation when the clock input and signal input have one quarter of period shift or 90^0 ($\pi/2$). For angles other than 90^0 , the output is not regular. The phase error voltage controls the VCO's frequency after being filtered by the loop filter. The filter used in PLL transforms the phase difference into an analog control voltage which is same as the average output of phase detector. The filter converts rapid variations of the phase detector output into a slow varying signal, which later controls the voltage controlled oscillator.

The most vital part of PLL is VCO which is used to produce clock in phase locked loop circuits. This unit ingests most of the power in the system in addition to operating at highest frequency i.e. the VCO reduces power

consumption. Although there are a variety of frequency synthesis techniques, phase locked loop (PLL) represent the dominant method in the wireless communications industry. PLL, like most wireless communication technologies, is relatively new and has matured only in the last decade.

The ability to execute all PLL functions on a single integrated circuit (IC) has created an economical, mass production solution to meet the needs of industry. Current PLL ICs are highly integrated digital and mixed signal circuits that operate on low supply voltages and consume very low power. To have very low power consumption, this work is decided to be implemented using VLSI technology.

II. SIMULATION SETUP

This paper describes the use of CMOS 45nm technology and the implementation of this technology in Microwind 3.1. In 45nm technology, required effective gate length is 25nm with metal gate and SiON gate dielectric. This technology is called “High speed technology” as it is devoted to applications for which the highest speed is the primary objective: fast microprocessors, fast DSP, etc.

The use of Software Microwind 3.1 is done in this paper which allows us to design and simulate an integrated circuit at physical description level. We can gain access to the Circuit Simulation by pressing one single key in this software .The electric extraction of the circuit is performed automatically and the voltage and current curves are produced by the analog simulator immediately.

III. EXPERIMENTAL RESULTS

Figure1.2. shows the layout of phase locked loop using 45nm technology. This PLL is designed with microwind 3.1 software using 45 nm design rule. Fig 1.3 shows the simulation result of Phase Locked Loop.

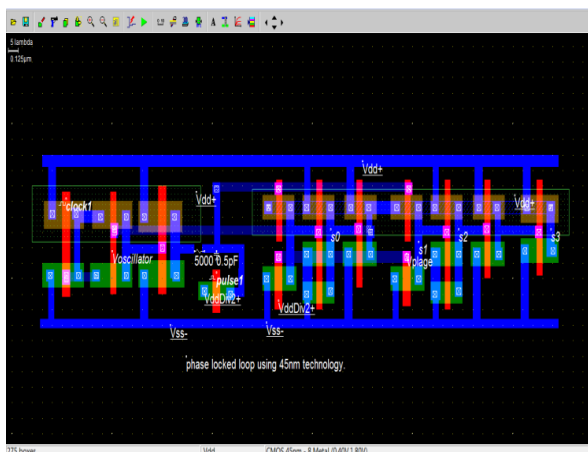


Fig 1.2 – Layout of PLL Using 45nm Technology

The simulation of a low power PLL is shown following figure 1.3 .This shows the simulation of a high performance PLL circuit, frequency versus time .The frequency is 5GHz. for which power consumed is 50.243 microwatt.

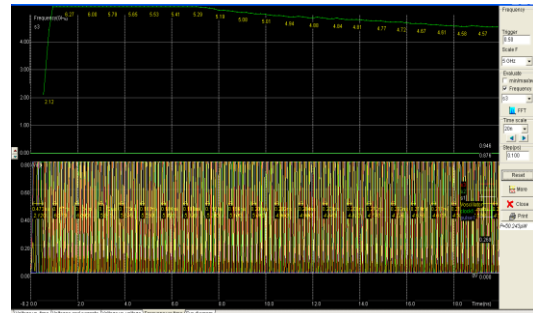


Fig: 1.3 -Simulation result of Phase locked loop (Frequency vs. Time)

IV. CONCLUSION

The main problem with PLL design using deep submicron technology is to gain low power consumption which may be due to the uncertainty in the value of threshold or supply voltage. As PLLs are extensively used in communication application such as frequency synthesis for missile tracking, noise stability is the most important factor which can be analysed with the components of filter. The Software microwind 3.1 used in this paper allows us to design and simulate an integrated circuit at physical description level.

We can gain access to Circuit Simulation by pressing one single key. The electric extraction of the circuit is automatically performed and the analog simulator produces voltage and current curves immediately. The layout of PLL which is developed in this paper is a modified design of low power high performance VCO. This is an optimum design for use in industries at 45 nm technology. In the estimated design, more emphasis is given on power consumption and layout design. This PLL consumes a very low power.

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BIOGRAPHIES



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