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Analysis of Discrete & Integrated Circuits for Piezoelectric Energy Harvesting

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Abstract: This paper discusses two circuits for piezoelectric energy harvesting; one is integrated circuit which consists of LTC®3588-1; a complete piezoelectric energy harvesting power supply, other one is a discrete circuit. Former one is simulated with the LTSPICE; later one is simulated in Proteus, and both the circuits are practically built and tested in laboratory. Based on the comparative study of these circuits, we suggest the use of integrated circuit in harvesting the mechanical energy (pressure) produced in shock absorbers of bike which could serve as an ancillary source of energy for charging mobile phone battery.

Keywords: Energy Harvesting, Piezoelectric transducer, Shock absorber, Battery charging, LTC 3588-1

I. INTRODUCTION

The term energy harvesting describes the process of converting ambient energy surrounding a system into useful electrical energy through the use of a specific material or transducer. Primarily, the selection of energy harvester as compared to other alternatives such as battery depends on two main factors, cost effectiveness and reliability.

In recent years, several energy harvesting approaches have been proposed using solar, thermoelectric, electromagnetic, piezoelectric etc. Piezoelectric Energy Harvesting is a new and innovative step in the direction of energy harvesting. It is attractive mainly due to the simplicity of piezoelectric transduction and the relative ease of implementation of piezoelectric systems into a wide variety of applications as compared to electrostatic or electromagnetic methods.

In this paper we are presenting two circuits for piezoelectric energy harvesting, one is integrated circuit which consists of LTC®3588-1; complete piezoelectric energy harvesting power supply. It integrates a low loss internal bridge rectifier with a synchronous step-down DC/DC converter. It uses an efficient energy harvesting algorithm to collect and store energy from high impedance piezoelectric elements, which can have short-circuit currents on the order of tens of mA. Other is a discrete circuit, which consists of a bridge rectifier, a storage capacitor, MOSFET & transistor for providing gain, and a voltage regulator. These two circuits are analyzed in terms of output voltage and current generated, and the results are compared. . Both of these circuits don't need any additional power supply for operation, and works completely on piezoelectric power.

II. BLOCK DIAGRAM OF ENERGY HARVESTING CIRCUIT

The basic block diagram of the proposed model is shown in Fig. 1. It consists of 5 main blocks:

(a) Piezoelectric transducer
(b) Rectifier
(c) Storage Capacitor
(d) Conditioning Circuit
(e) Regulator.

AC voltage is generated from the piezoelectric transducer proportionate to the amount of deformation in the transducer which is rectified by the rectifier block and then it is stored in a storage device such as a battery.

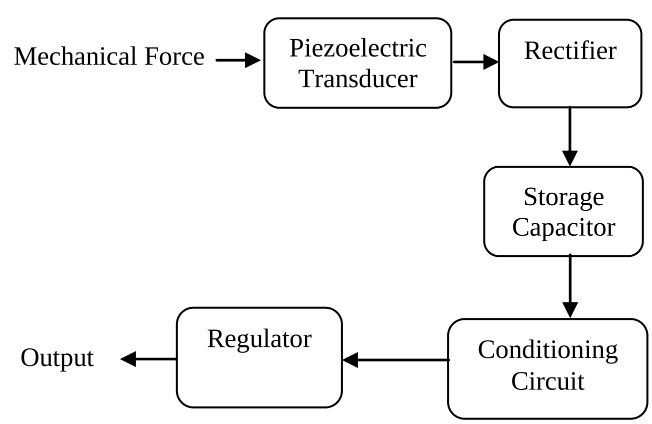

Fig. 1 Basic Block Diagram of Piezoelectric Energy Harvesting circuit

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III. INTEGRATED CIRCUIT

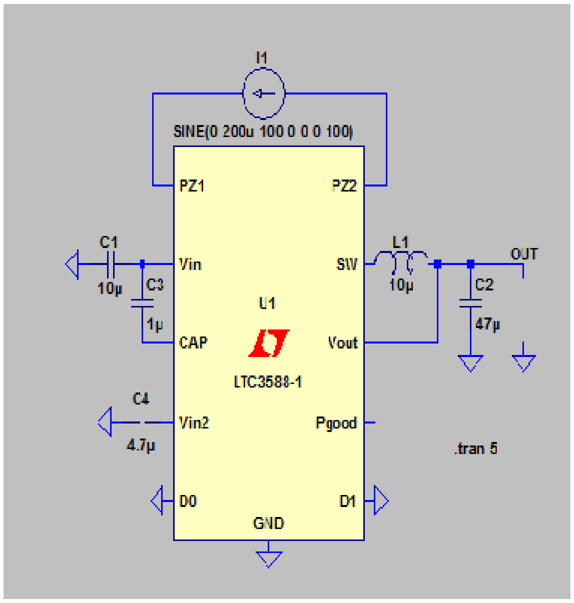

Fig. 2 LTC 3588-1 biasing circuit

A. Component & Working:

- C1= $C_{storage}$ =10uF: This Capacitor is connected between V_{in} & GND. The rectified output is stored on this capacitor and can be used as an energy reservoir for the buck converter (present inside LTC 3588-1)
- C2= 47uF: It is connected at the output. This capacitor also acts as an energy reservoir. It is continuously discharged during load condition.
- C3= 1uF: It is connected to the CAP and VIN2 pins to serve as energy reservoirs for driving the buck switches.
- C4= 4.7uF: It is connected between Vin2 and GND. It also serves as energy reservoirs for driving the buck switches.
- Inductor L1= 10uH: The buck converter is optimized to work with an inductor of 10uH.
- D1: Output Voltage Select Bit. D1 should be tied high to VIN2 or low to GND to select desired V_{OUT} .
- D0: Output Voltage Select Bit. D0 should be tied high to VIN2 or low to GND to select desired V_{OUT}

TABLE I
BIT SETTING FOR CONFIGURING OUTPUT VOLTAGE

D1	D0	o/p voltage
0	0	1.8 V
0	1	2.5 V
1	0	3.3 V
1	1	3.6 V

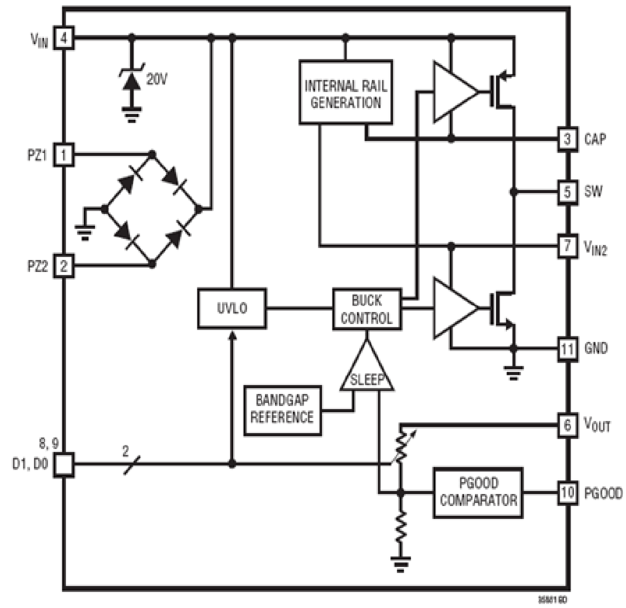

Fig. 3 Internal Block Diagram of LTC 3588-1

- Internal Bridge Rectifier:

The LTC3588-1 has an internal full-wave bridge rectifier accessible via the differential PZ1 and PZ2 inputs that rectifies AC inputs such as those from a piezoelectric element. The rectified output is stored on a capacitor at the VIN pin and is used as an energy reservoir for the buck converter.

- Under Voltage Lockout (UVLO):

When the voltage on VIN rises above the UVLO rising threshold the buck converter is enabled and charge is transferred from the input capacitor to the output capacitor. When the input capacitor voltage is depleted below the UVLO falling threshold the buck converter is disabled.

- Internal Rail Generation:

Two internal rails, CAP and VIN2, are generated from VIN and are used to drive the high side PMOS and low side NMOS of the buck converter, respectively. Additionally the VIN2 rail serves as logic high for output voltage select bits D0 and D1. Capacitors are connected to the CAP and VIN2 pins to serve as energy reservoirs for driving the buck switches.

- Buck Operation:

The buck converter charges an output capacitor through an inductor to a value slightly higher than the regulation point. It does this by ramping the inductor current up to 260mA through an internal PMOS switch and then ramping it down to 0mA through an internal NMOS switch. This efficiently delivers energy to the output capacitor.

If the input voltage falls below the UVLO falling threshold before the output voltage reaches regulation, the buck converter will shut off and will not be turned on until the input voltage again rises above the UVLO rising threshold.

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When the buck brings the output voltage into regulation the converter enters a low quiescent current sleep state that monitors the output voltage with a sleep comparator. During this operating mode load current is provided by the buck output capacitor. When the output voltage falls below the regulation point the buck regulator wakes up and the cycle repeats.

- Power Good Comparator:

A power good comparator produces a logic high referenced to V_{OUT} on the PGOOD pin the first time the converter reaches the sleep threshold of the programmed V_{OUT}, signalling that the output is in regulation. The PGOOD pin will remain high until V_{OUT} falls to 92% of the desired regulation voltage.

IV. DISCRETE CIRCUIT

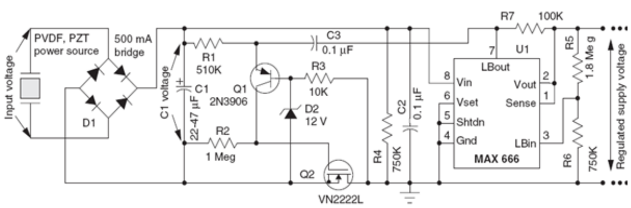

Fig. 4 Discrete Circuit

A. Design of Discrete Circuit:

1.) Piezoelectric Transducer:

- Output Voltage: 0-15 V
- Output Current: 15-20uA

2.) Bridge Rectifier (Diodes):

- 1N4148: Fast switching diodes are used since the Frequency of operation of piezoelectric transducer is high.
- Repetitive peak reverse voltage: 100V (max)

3.) Transistor: 2N3906 (PNP Switching Transistor)

h_{FE} = 300(max)

Biasing of Transistor:

Resistors:

R1= R_E = 1MΩ

R2= R_C = 510KΩ

This is a DC biasing since there is no input signal. The coordinates of operating point (V_{CEQ}, I_{CQ}) selected as (9V, 2uA).

Applying KVL to above circuit:

$$V_{CC} - V_{CEQ} - I_{CQ} *(R_C + R_E) = 0$$

$$12V - 9V - 2uA * (R_C + R_E) = 0$$

$$(R_C + R_E) = 1.5 \times 10^6$$

Let R_C = 1MΩ

Therefore R_E = 500K

4.) Zener Diode: A zener Diode (D2) of 12V is clamped between the base of the transistor and ground. Therefore the transistor will come into conduction only when the supply voltage reaches 12.6V. (The Z1 breakdown voltage plus the drop across the base-emitter junction of Q1).

5.) MOSFET : VN2222L (N channel Enhancement type switching MOSFET)

$V_{GS(th)}$: 2V (min)

The drop across the Collector resistor is given as V_{GS} to the MOSFET. Therefore when the drop across this resistor reaches 2V the MOSFET turns on.

Drop across R_C is calculated as:

$$V_{RC} = I_{CQ} \times R_C$$

$$V_{RC} = 2uA \times 1M\Omega$$

$$V_{RC} = 2V$$

6.) MAX 666 Voltage Regulator:

- Operating Range: 2V -16.5V
- Output Current: 40mA
- Dual Mode Operation: Fixed 5V or Adjustable from 1.3V- 16 V
- Here we have designed this regulator to provide fixed 5V output. Therefore the V_{SET} pin is grounded.
- Since the current limiting is not used the SENSE pin is connected to V_{OUT}.
- MAX666 contains on chip circuitry for low battery or low power supply detection. If the voltage at L_{BI} (pin3) falls below the regulators internal reference (1.3V), then L_{BO} (pin7) is grounded momentarily.

The Threshold can be set to any level above the reference voltage by connecting a resistive divider to LBI.

Design Equation:

$$R5 = R6 \times \left(\frac{Vbat}{1.30\ V} - 1\right)$$

Where V_{bat} is the desired threshold of low battery detector and R5 & R6 are LBI input divider resistors

For our design we have taken V_{bat} to be 4.5V.

Hence $$R5 = R6 \times \left(\frac{4.5\ V}{1.30\ V} - 1\right)$$

$$R5 = R6 \times (2.46)$$

Let R6= 750KΩ

Therefore R5 = 1.846MΩ

7.) Capacitors:

C1= 22uF: This acts as a storage capacitor and provides supply to all other components.

C2=C3= 0.1uF

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All the capacitors used are electrolytic.

B. Working:

- The signal from the piezoelectric source is full-wave rectified through a diode bridge D1. As the source signal ramps up, charge transfers to electrolytic bucket capacitor C1 whenever the source voltage overcomes the voltage already supported by this capacitor (plus two diode drops).
- As C1 charges beyond 12.6 V (the Z1 breakdown voltage plus the diode drop across the base-emitter junction of Q1), Q1 is forced into conduction, in turn activating Q2 and latching Q1. With Q1 on, the high side of C1 now has a current return path to ground and discharges through the Maxim MAX666.
- The regulator is biased to provide a stable +5 V supply, as long as C1 has sufficient charge to produce a valid regulator output voltage (V_{out}).
- When V_{out} swings below approximately 4.5 V (as set by R5 and R6), the low battery in pin (LB_{in} on U1) is pulled below its threshold, driving the low-battery out pin (LB_{out}) to ground momentarily. This negative pulse through C3 turns Q1 Off, thus deactivating Q2 and renewing the C1 charging cycle.

V. RESULTS

A. Integrated Circuit

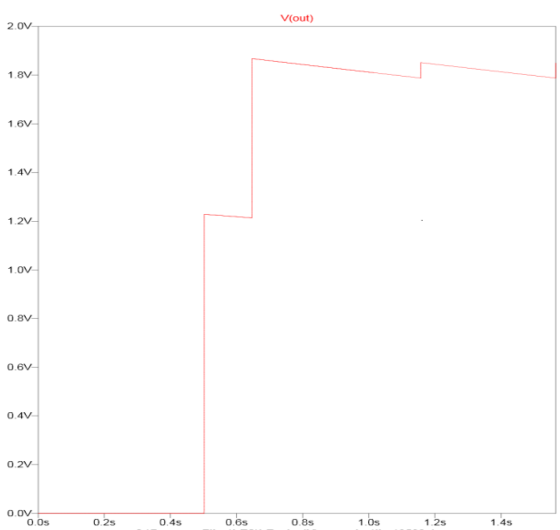

Fig. 5 Output Voltage vs. Time (simulated in LTSPICE)

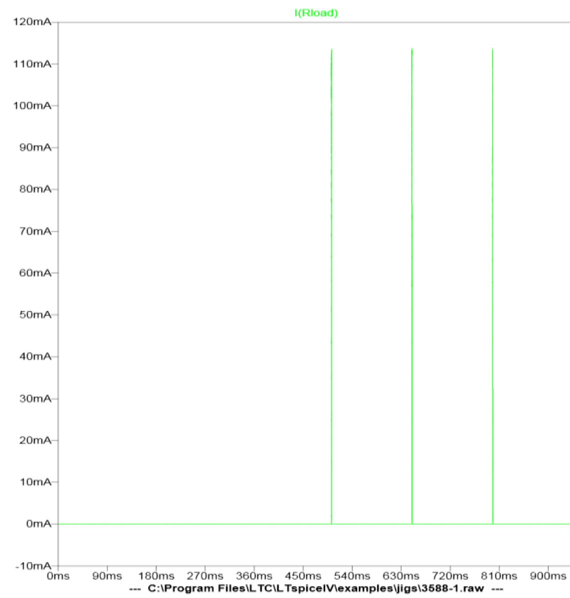

Fig. 6 Output Current vs. Time (simulated in LTSPICE)

B. Discrete Circuit

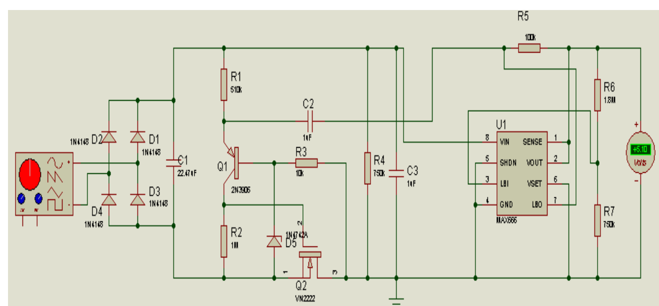

Fig. 7 Proteus simulation of discrete circuit

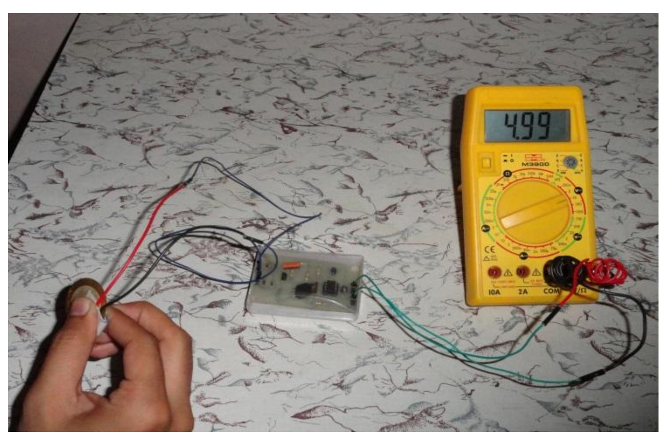

Fig. 8 Experimental setup of discrete circuit

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TABLE II
OBTAINED RESULTS

Parameter	**Discrete**	**Integrated**
Current	4mA	60 mA
Voltage	5V	3.6 V(configured)

VI. CONCLUSION

Thus it is concluded that the performance of Integrated circuit is much better than that of Discrete Circuit. Also, Integrated circuit puts back the Discrete Circuit in terms of cost, size and reliability. We propose to use the Integrated circuit in shock absorbers of bike. A piezoelectric device can be mounted on the spring assembly for generating electrical energy in response to strain imposed thereon in response to the compressions and extensions of the spring assembly. This energy can then be used for charging a mobile phone battery.

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