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Block Formulated Efficient Reconfigurable Interpolation Filter

Akhil S R.[1], Pramod P.[2]

Student, M.Tech, VLSI Design & Signal Processing, LBS College of Engineering, Kasaragod, Kerala, India[1]

Assistant Professor, ECE Department, LBS College of Engineering, Kasaragod, Kerala, India[2]

Abstract: Interpolators are used in digital signal processing systems to increase the sampling rate. An interpolation filter consist of an input matrix and coefficient matrix with up-sampling factor P and filter length N. Interpolation filter has different coefficient vector for different up-sampling factors. Here interpolation filter architecture is designed for different up-sampling factors. Reuse of partial results in reconfigurable filter for eliminating redundancy in computation.Parallel computation is performed by block formulation method. Reconfigurable Interpolation filter is implemented using VHDL language by Xilinx software. A ripple carry adder is used in filter architecture for performing addition operation. A block formulated reconfigurable architecture is presented for area, delay and power efficient realization of interpolation filter.

Keywords: Interpolation, Reconfigurable, VLSI.

I. INTRODUCTION

In Digital Signal Processing (DSP) systems interpolators are used to increase the sampling rate. Interpolators consist of an up-sampler to change the sampling rate of baseband signal and an anti-imaging (interpolation) filter to suppress the unwanted interference effect caused by up-sampling the baseband signal. Commonly pulse shaping filters like root raised cosine (RRC) filter is used as interpolation filter. RRC filter has high inter-symbol interference (ISI) rejection ratio and high bandwidth limitation. When up-sampling factor of a baseband signal changes coefficient vector of interpolation filter also changes. Software Defined Radio is used in transmitter-receiver section of wireless communication. Efficient reconfigurable FIR filter hardware is realized by either multiplier or multiplier less design. An efficient interpolation filter is also be designed for different up-sampling factor of filter length N. In which block formulation method is used for parallel processing Reconfigurable interpolation filter is designed by reuse of partial results for different up-sampling factors. Interpolation filter involves an input matrix and coefficient matrix. When up-sampling factor P changes the size of input matrix changes. So here a single interpolation filter structure can perform operation for three up-sampling factors. Reuse of partial products helps for the removal of redundant computations and parallel processing is performed with block formulation method.

Single rate interpolation filter is described in [2]. Which has a single fixed up-sampling factor .Interpolation filter operates at P up-sampling factor with filter length N. Area efficient pulse shaping filter based interpolation filter is introduced in [3]. It can't use for reconfigurable application more than P=4.LUT based interpolation filter is proposed in [4]. LUT decomposition scheme is used in filter and it cannot be reconfigures for up sampling factors other than P=4. It has less area complexity. DA based reconfigurable interpolation filter is used in [5]. DA-LUT stores partial results of all sub –filter outputs. This architecture is reconfigured for different interpolation factors. This interpolation filter architecture has features such as elimination if redundancy and producing multiple outputs without reconfiguration. The synthesized result shows that this architecture has less area, delay and area-delay product (ADP).

Interpolation is essential when there is a need of changing from one sampling rate to another. It is also called as up-sampling in which inserting zero valued samples between original input data samples to increase the sampling rate. A reconfigurable FIR interpolation filter is suitable for power constrained multi-standard SDR receiver. In this work a new parallel multiplier based reconfigurable structure is described for interpolation filter.

The rest of this paper is as follows section II describes proposed method of interpolation filter architecture. In section IIIresult analysis is described.Finally, conclusion is described in section IV.

II. PROPOSED METHOD

The proposed structure for area –delay efficient reconfigurable interpolation filter is shown in figure 1 for block size of L=4 and filter length N=16. It consists of one input vector generation unit, one arithmetic unit, one coefficient selection unit.Block processing helps for the low power implementation of filters. A parallel reconfigurable architecture can be designed using the partial result generation unit and the reconfigurable adder unit. The working flow is described as

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follows. Based on the filter specification, co-efficient are first generated by using the Filter Design. Next the filter specifications are applied to the register arrays and produce the input vectors. At first these input vectors and coefficients are multiplied. Then the multiplied outputs are added together to get the final output.

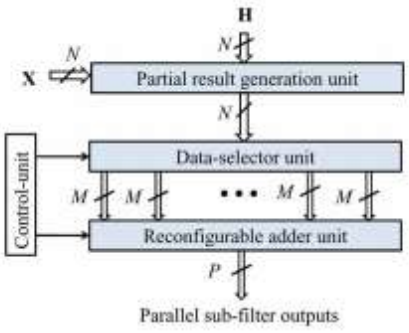

Fig. 1. Reconfigurable interpolation filter

The Vector Generation Unit (VGU) receives one input-block in each cycle and generates input-vectorseach in parallel. Architecture of the VGU is shown in figure 2. It is comprised of (N-1) registers. The VGU receives a block of input samples in every cycle, produces 8 data-vectors in parallel. The block of inputs is determined by using the block formulation method.

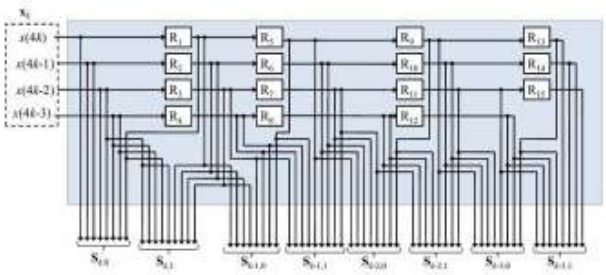

Fig. 2. Vector Generation Unit

The structure of Arithmetic Unit (AU) is shown in figure 3 having interpolation factors (IF2, IF4, IF8) and for block size L=4, and filter length N=16.

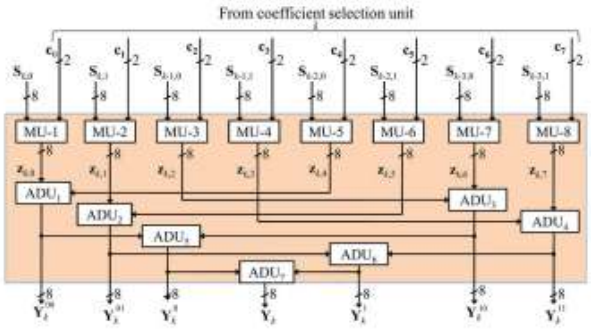

Fig. 3. Arithmetic Unit

Arithmetic unit is comprised of Multiplier Units (MUs) and Adder Units (ADU) it is shown in figure 4.N/P1 number of Multiplier Units and (N/P1)-1 number of Adder Units.Each Multiplier Unit receives an LP1 point input-vector from the VGU and a short P1-point coefficientvector Cm from the CSU, and calculates one partial filter output-vector.

The partial output-vectors (Zk,0, Zk,4), (Zk,1, Zk,5), (Z k,2, Zk,6) and (Zk,3, Z k,7) added in four separate ADUs (ADU1, ADU2, ADU3, ADU4) to compute filter output-blocks (Y 00 k , Y 01 k , Y 10 k , Y 11 k) of IF8. For IF4, the output-vectors (Y00 k, Y01 k, Y10 k, Y11 k)represent its partial filter output. The adders ADU5 and ADU6 add the partial output-vectors. As a result the complete filter output vectors of IF4 (Y0k, Y1k). Similarly, the output vectors of IF4 represent the partial filter outputs of IF2. Then these output vectors are added in ADU7 to get the output vector Yk of IF2.

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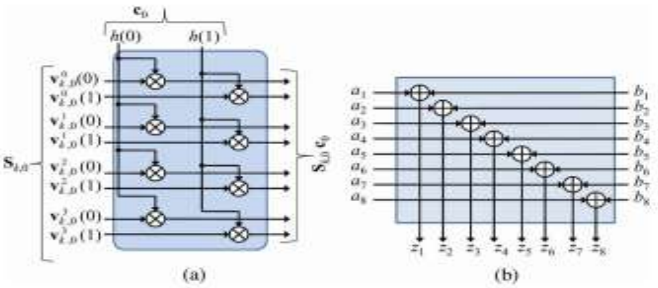

Fig. 4. (a) Multiplier unit. (b) Adder unit

Here Ripple Carry Adder is used to perform the addition operation in arithmetic unit. Multiple full adder circuits can be cascaded in parallel to add an N bit number. A ripple carry adder is a logic circuit in which the carry output of each full adder is the carry in of the succeeding next most significant full adder. It is called ripple carry adder because each carry bit gets rippled into the next stage. A standard 8 bit ripple carry adder built as a cascade from eight 1 bit full adder. Consider a 8 bit ripple carry adder delay, area and power consumption of reconfigurable interpolation filter is reduced. Figure 5 shows block diagram of ripple carry adder.

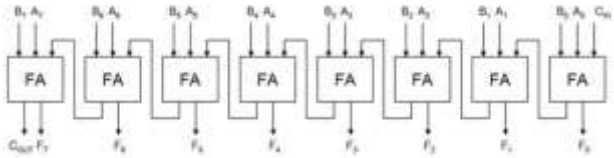

Fig. 5. Ripple Carry Adder

III.RESULT ANALYSIS

The three basic modules are synthesized using VHDL in Xilinx ISE web pack 14.1. Then simulated using Modelsim SE 10.3c simulator.With the help of VHDL language interpolation filter architecture can be done for reconfigurable applications with ripple carry adder for addition operation. Filter simulation output for filter length 16 and block size of 4 is shown below. We obtained filter output for block of L=4. 8 bit ripple carry adder is used for computing addition operations.. The delay, area and power can be measured with help of cadence tool and comparison is performed. Table1, figure 5, figure 6, figure 7, shows the performance comparison between reconfigurable interpolation filter architecture with reconfigurable interpolation filter with Ripple carry adder. The comparison is performed based on parameters such as area, delay and power. Interpolation filter with ripple carry adder is efficient compared with interpolation filter with normal addition in terms of area, delay and power for reconfigurable application for block size of L=4, and filter length of 16.

Table 1 Performance comparison

Parameters	Reconfigurable interpolation filter	Interpolation filter with ripple carry adder
Delay (nS)	8.77	4.05
Power (mW)	695.83	29.99
Cell Area($x10^3$)	1880.32	163.17

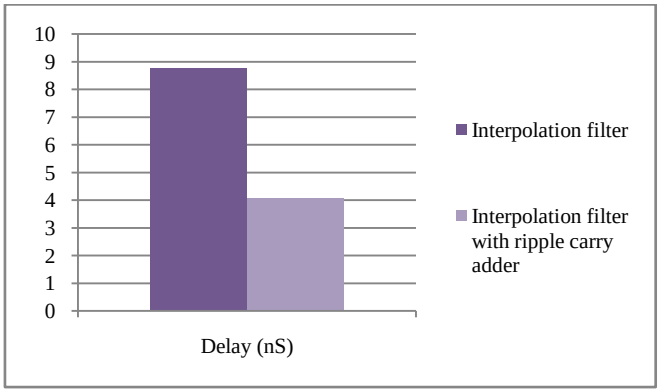

Fig. 6. Delay comparison

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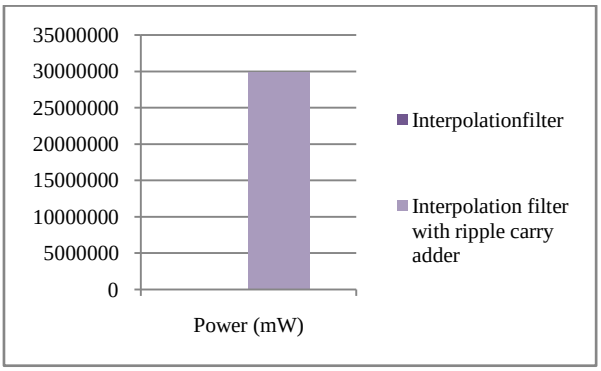

Fig. 7. Power comparison

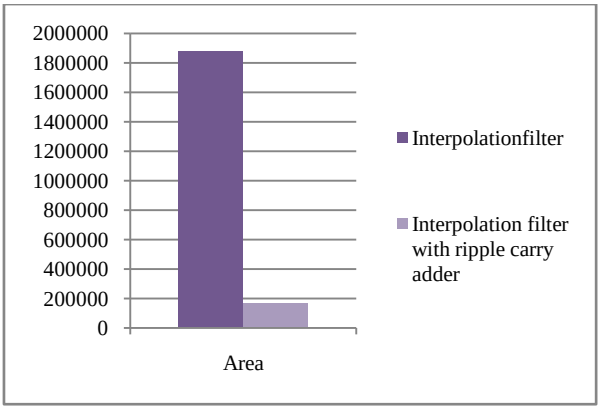

Fig. 8. Area comparison

IV. CONCLUSION

In this Reconfigure interpolation filter architecture, the partial results are reused for parallel computation of filter outputs of different up-sampling factors. It does not require reconfiguration to compute filter outputs of a particular interpolation filter for different up-sampling factors, and configured when there is a need to change the filter specification. In that case, a coefficient-vector of the desired filter is selected from the CSU and fed to the AU to perform the filter computation. The VGU and AU constitute the main part of this structure. They do not require any reconfiguration to change the filter computation. Therefore, the proposed architecture offers reconfigurable without using any overhead complexity unlike the existing reconfigurable architectures. This filter outputs at multiple sampling frequency for an input sampling frequency is a unique feature of this architecture. The complexity of this architecture is independent of up-sampling factor and it does not increase proportionately with the blocks-size. Therefore the area-delay efficiency of the proposed architecture is expected to be better for higher blocksizes. The entire architecture can be designed using VHDL language and synthesized Xilinx ISE web pack 14.1 and simulated in ModelSim SE 10.3c.

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