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A New Multilevel Voltage Source Inverter with SPWM for Medium Voltage Application

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Abstract: This paper introduces a new Five-Level Voltage Source Inverter (VSI) for medium voltage high-power applications.This VSI can operate over an extensive variety of voltages and it has higher quality output voltage waveform and less quantity of components. Two methods are used to generate an output level, to control and adjust the flying capacitors to their coveted values. In the first method a simpleSPWM scheme is used by the comparing sinewave with output levels and second method involves comparison between sine wave with triangular signals. Second method gives better performance. The proposed five level converter is simulated in MATLAB/Simulink environment.

Keywords: Multilevel converter, Sinusoidal Pulse Width Modulation (SPWM), DC–AC power conversion.

I. INTRODUCTION

Multilevel inverter technology has risen as one of the essential substitute in the high power medium voltage energy control. There are predetermined number of topologies that give multilevel voltages and are appropriate for high power and medium voltage applications, this is because multilevel topologies can synthesize near sinusoidal voltage with low harmonic distortion that moderates the size of output filter. These topologies have likewise decreased common mode voltage, low switch stress and high voltage ability [1].

The advanced converter topologies which have been marketed effectively by real producers are the Diode Clamped Converter (DCC), the Flying capacitor (FC), and the Cascaded H-Bridge Multilevel Converters. There are different topologies, for example, hybrid converters, but they are not completely acknowledged for industrial applications. However, these topologies confine their applications for higher levelsdue to their drawbacks [4].

Many researches have discussed about various new multilevel converters for more levels [4-10]. There arethree major multilevel topology variations which have been indicated by them;among the existing topologies, the below topologies with five-level structure have found practical applications; the five-level H-bridge NPC (5L-HNPC) and the five-level Active NPC (5L-ANPC). The main features of these converters are:

The H-bridge connection of two classic 3L-NPC phase legs yields a five-level H-bridge NPC (5L-HNPC). This topology incorporates three isolated dc sources which is fed by a phase shifting transformer and various diode bridges. The bulky phase shifting transformer additionally expands complexity and cost of the converter [5].

The combination of a 3L-ANPC and 3L-FC yields a Five-Level Active NPC (5L-ANPC), which increments the voltage levels. More number of output levels can be acquired by this converter. The voltage rating of the power semiconductors are distinctive in 5L-ANPC and it is the fundamental disadvantage; the outer switches are subjected to half of the dc-link voltage but the inner devices have only one fourth of the dc-link voltage. This restricts the voltage rate of the converter for higher voltage applications [6].

A Five-Level Diode-Clamped Converter which has an extensive number of clamping diodes. This converter has 36 diodes, 12 diodes in each phase. Voltage adjusting of the dc-link capacitors is another issue with this topology [4].

A Five-Level Flying Capacitor (FC) Converter. In this converter there are two main issues; the number of flying capacitor and regulating voltages of the flying capacitors. The quantity of capacitors are attempted to diminish by the manufacturers in practical applications [5].

As proposed in [10], A New Nested Neutral Point Clamped (NNPC) converter, where voltage stress across each switch is same (equal to 1/3rd of the dc voltage), when comparedwith other classic four-level topologies it has fewer components [10].

Another Five-Level Voltage Source Converter is developed in this paper, which depends on the redesign of a four-level NNPC converter. The operating voltage of this inverter is of overwide range without the need of power semiconductor that are connected in series and it also has less components. This five-level converter overcomes the downsides of the previous five-level converters.

A simple SPWM strategy is used for the new converter to control and balance or adjust the capacitor voltages. Using the MATLAB/Simulink environment the performance of the converter is investigated.

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2. CONVERTER TOPOLOGY

2.1. Operation of the Proposed Five-Level Voltage Source Inverter

The proposed multilevel converter topology is as shown in Figure 1. The capacitor Cx_1 and Cx_2, x=phase a, b, c are charged to one-fourth of Vdc ($1/4^{th}$Vdc) and Cx_3 is charged to three-fourth of Vdc ($3/4^{th}$Vdc) to ensure equally spaced steps in the output voltages.

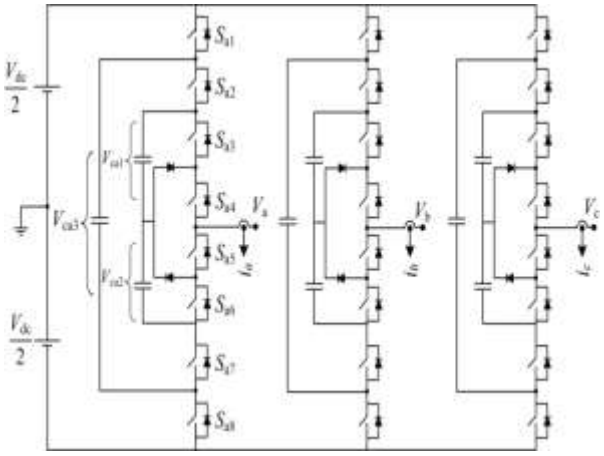


Figure 1: A new five-level three-phase inverter

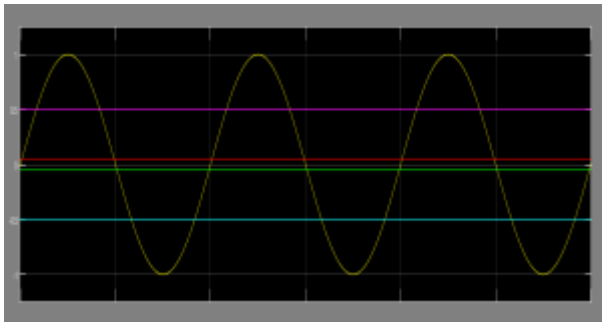
Five output levels are accomplished with the twelve distinct switching combinations. The switching combinations list is shown in Table I. It should be noticed that the voltage stress over the switches do not go beyond 1/4th of dc-link voltage. The repetitiveswitch combination to produce the output levels is another preferred standpoint of this converter topology. For instance, there are 3 excessive switching states (from Table I) to generate voltage levels of $1/4V_{dc}$ and $-1/4V_{dc}$ and there are 4 excessive switching states to generate voltage levels of two. For each floating capacitor each repetitivestate provides a charging and discharging current path. Voltage balancing of the capacitors are achieved by this component of repetitiveswitching states.

2.2. SPWM Scheme for the Proposed Multilevel Inverter

Sinusoidal PWM (SPWM) is a standout amongst the most well known modulation scheme in industrial applications. Two methods have been used to generate multilevel output voltage. In the first method modulation scheme is based on comparing sinewave and output levels and in second method modulation scheme is based on comparing sinewave and triangular signal. A multicarrier SPWM strategy is used to generate multilevel output voltage while adjusting the flying capacitors voltage, in this employing the deviation of the capacitor voltages from their nominal values and depending on the converter outputcurrent the best switching state is selected from the available excessive switching states to charge or discharge the capacitors and finally regulate the voltages of capacitors. This method of approach is intuitive and simple to implement in a digital control system.

Fig. 2(a) shows the desired output levels which is the result of comparing (1) sinewave and output levels and (2) sinewave and triangular signal Fig. 2(b).With respect to the desired level at the output, and from Table I the corresponding switching state can be chosen and then applied to the power switches.

(1) Sinewave and output levels



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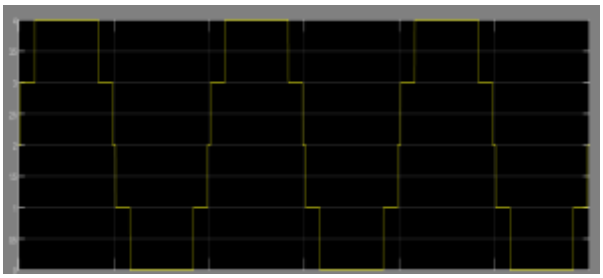


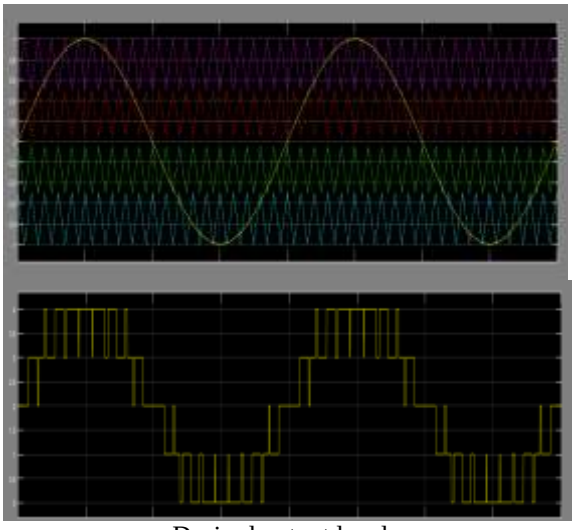
Desired output levels

Fig.2(a). comparing sinewave and output levels

Table I: Different switching states of the Five-Level Converter

State	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	V_{Cx1}		V_{Cx2}		V_{Cx3}		V_{ax}	Level
									i_x >0	i_x <0	i_x >0	i_x <0	i_x >0	i_x <0		
E	1	1	1	1	0	0	0	0	-	-	-	-	-	-	V_{dc} / 2	4
D3	1	1	0	1	1	0	0	0	C	D	-	-	-	-	V_{dc} / 4	3
D2	0	1	1	1	0	0	0	1	-	-	-	-	D	C		
D1	1	0	1	1	0	0	1	0	D	C	D	C	C	D		
C4	1	1	0	0	1	1	0	0	C	D	C	D	-	-	0	2
C3	1	0	0	1	1	0	1	0	-	-	D	C	C	D		
C2	0	1	0	1	1	0	0	1	C	D	-	-	D	C		
C1	0	0	1	1	0	0	1	1	D	C	D	C	-	-		
B3	0	0	0	1	1	0	1	1	-	-	D	C	-	-	$-V_{dc}$ / 4	1
B2	1	0	0	0	1	1	1	0	-	-	-	-	C	D		
B1	0	1	0	0	1	1	0	1	C	D	C	D	D	C		
A	0	0	0	0	1	1	1	1	-	-	-	-	-	-	$-V_{dc}$ / 2	0

(2) Sinewave and triangular signal



Desired output levels

Fig.2(b). comparing sinewave and output levels

Table I shows the excessive switching states for level 1, 2 and 3, and also it is observed that each redundancy state depending on the sign convention of output current can charge or discharge the flying capacitors and the difference

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between the nominal voltage values and the measured voltage values are limited. For instance, when the desired output level is 1 and the capacitor Cx3 needs to be charged, if the output current is positive the switching state B2 should be chosen to charge the capacitor Cx3 and if the output current is negative the switching state B1 should be chosen.
If there is no control over the currents that flow into/out from the flying capacitors to charge/discharge the capacitors, therefore the voltage of the flying capacitors may deviate from their desired values.
The voltage deviation of the flying capacitors can be expressed as:

$$\Delta Vcxi = Vcxi - Vcxi,$$

$$x = \text{phase a,b,c, and } i = 1,2,3 \ldots\ldots\ldots (1)$$

where V_{Cxi} are the capacitor voltages, $V_{cxi,\ ref}$ are the nominal values which Vcxi, ref = Vdc / 4 for i=1,2 and Vcx3, ref = 3Vdc / 4.
It can be seen from the Table I, to charge and discharge the flying capacitors, there are enough redundancy at level 1, 2 and 3. Table II shows that which switching state should be chosen in different conditions to control voltage of flying capacitors. For instance, if the level is 1 and the deviation of capacitor Cx2 is more than Cx3 ($|\Delta VCX2| > |\Delta VCX3|$), it means that the main priority should be given to charge or discharge capacitor Cx2. Assume that ix> 0, if $\Delta Vcx2 > 0$, therefore the capacitor Cx2 should be discharged and thus the state B3 should be selected.

Table II: The voltage balancing method for each phase of the five-level inverter

Output Level	Condition	i_x	$\Delta VCX1$	$\Delta VCX2$	$\Delta VCX3$	State
3	|ΔVCX1| > |ΔVCX3|	≥ 0	≥ 0	-	-	D1
			< 0	-	-	D3
		< 0	≥ 0	-	-	D3
			< 0	-	-	D1
	|ΔVCX3| > |ΔVCX1|	≥ 0	-	-	≥ 0	D2
			-	-	< 0	D1
		< 0	-	-	≥ 0	D1
			-	-	< 0	D2
2	|ΔVCX1| > |ΔVCX3| & |ΔVCX1| > |ΔVCX2|	≥ 0	≥ 0	-	-	C1
			< 0	-	-	C2 / C4
		< 0	≥ 0	-	-	C2 / C4
			< 0	-	-	C1
	|ΔVCX2| > |ΔVCX1| & |ΔVCX2| > |ΔVCX3|	≥ 0	-	≥ 0	-	C3 / C1
			-	< 0	-	C2
		< 0	-	≥ 0	-	C2
			-	< 0	-	C3 / C1
	|ΔVCX3| > |ΔVCX1| & |ΔVCX3| > |ΔVCX2|	≥ 0	-	-	≥ 0	C2
			-	-	< 0	C3
		< 0	-	-	≥ 0	C3
			-	-	< 0	C2
1	|ΔVCX2| > |ΔVCX3|	≥ 0	-	≥ 0	-	B3
			-	< 0	-	B1
		< 0	-	≥ 0	-	B1
			-	< 0	-	B3
	|ΔVCX3| > |ΔVCX2|	≥ 0	-	-	≥ 0	B1
			-	-	< 0	B2
		< 0	-	-	≥ 0	B2
			-	-	< 0	B1

Procedure to be followed to control the flying capacitor voltages (with respect to Table I&II):

1. By comparing carrier and modulation signal the desired output level should be determined.
2. Depending on the sign convention of the phase current and voltages of the flying capacitors ought to be measured and then the capacitor voltage deviation can be determined depending on step 1,

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3. The suitable switching state can be chosen from Table II and the corresponding gating signals will be applied to the power semiconductors.

The procedure to control voltage of flying capacitors in each phase is as follows. Initially the modulating signal for x (x=phase a,b,c) is compared to carriersand then the corresponding output levels are decided.If the desired output level(L) is 1, 2 or 3, the parallelswitching state will be State B, C or D, in the same way if the level 0 or level 4 is the desired output level (L), the parallel switching state will be State A or E from Table I respectively. On the other hand, the capacitor voltages (VCX1, VCX2 and VCX3) and phase current (i_x) should be measured and then based on the output level (L) the convenient switching state should be selected from Table II.
For each leg, this procedure can be applied separately for flying capacitor voltages control, the only difference is that modulating signals should have $\pm 120^o$ phase shift respect to each other.

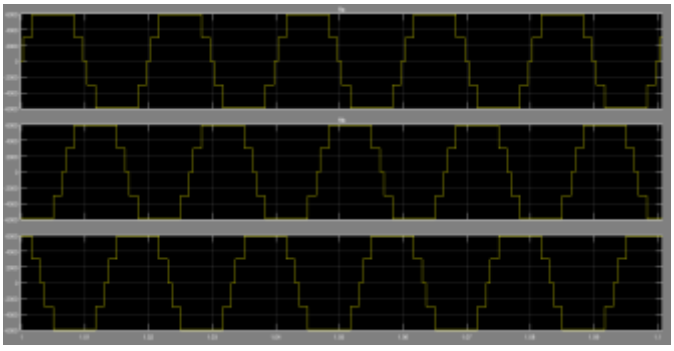
3. SIMULATION RESULTS

To demonstrate the execution of the Five-Level converter, simulation studies have been carried out in MATLAB/Simulink tool. Table III shows the parameters of the system utilized in simulation studies. The simulation also exhibits the adequacy of the used SPWM to generate output voltages and to regulate and adjust the voltage of flying capacitors. The performance of the proposed five-level converter and SPWM controller has been studied for different loads.

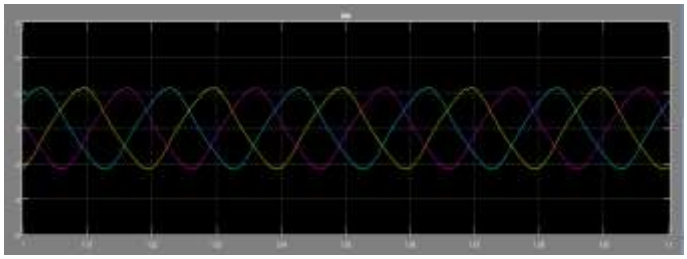
Table III: parameters of the study system (simulation)

Converter Parameters	Values
Flying Capacitors	1000 µF
Input DC Voltage	12 kV
Output Frequency	50 Hz
Device Switching Frequency	500 Hz

(1) Comparing sinewave and output levels
(a) Inverter output voltage (kV)



(b) Output currents (A)



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(c) Flying capacitors voltages (kV)

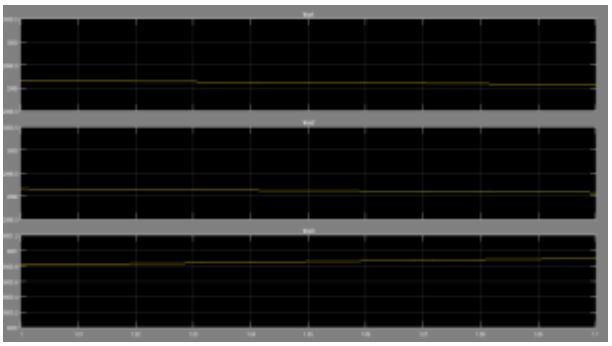
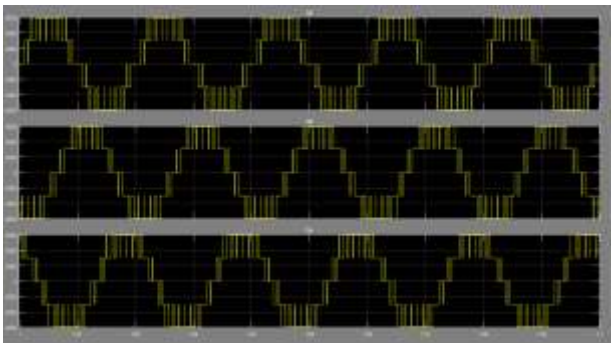
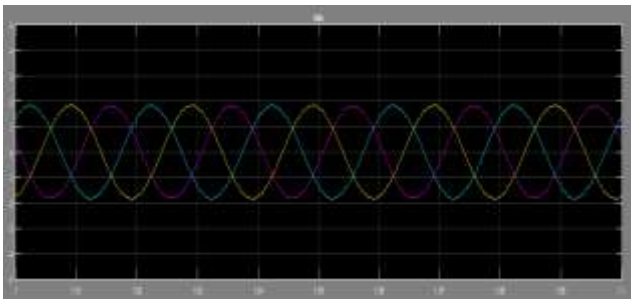


Fig. 3. Simulation waveforms (Resistive load)
(a) Inverter output voltage, (b) output currents, and (c) flying capacitors voltage.

(2) Comparing sinewave and triangular signal.
(a) Inverter output voltage (kV)



(b) Output currents (A)



(c) Flying capacitors voltages (kV)

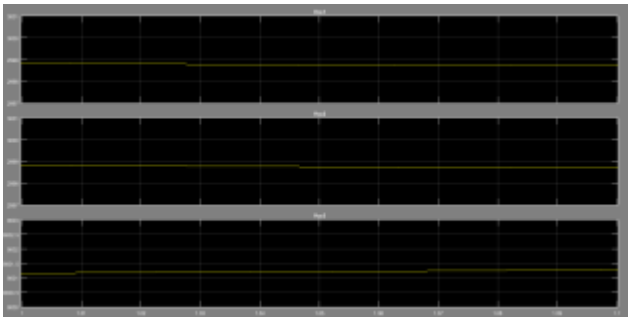


Fig. 4. Simulation waveforms (Resistive load)
(a) Inverter output voltage, (b) output currents, and (c) flying capacitors voltage

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4.1 Total Harmonic Distortion (THD) Analysis:
Based on sinewave and output levels:

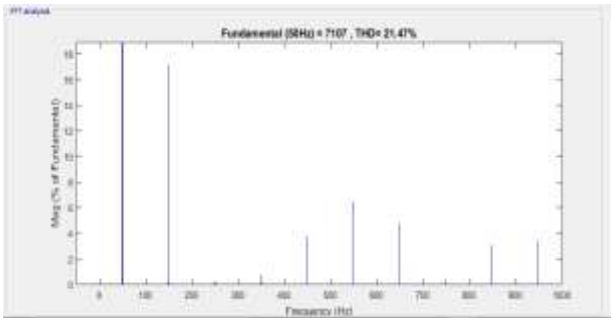

Fig.5. THD Analysis of output voltage

It indicates the fundamental component present in the output voltage is 7107V and the THD is 21.47%.

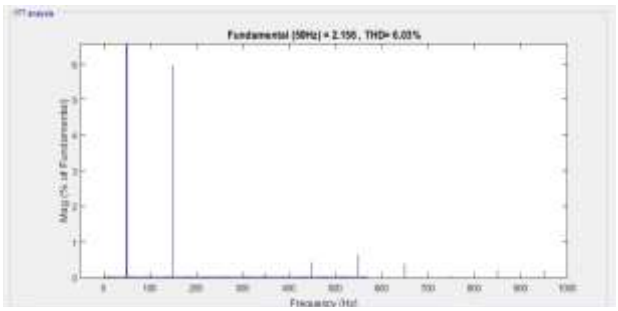

Fig.6. THD Analysis of output current

It indicates the fundamental component present in the output current is 2.156A and the THD is 6.03%.

Based on sinewave and triangular signals:

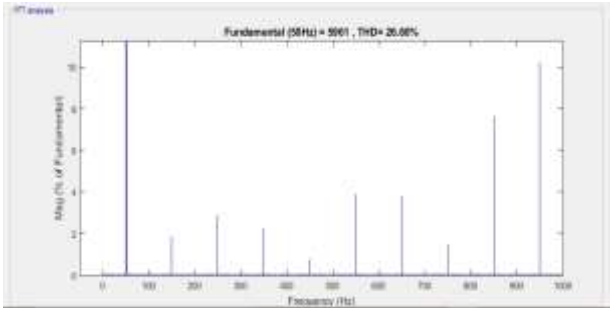

Fig.7. THD Analysis of output voltage

It indicates the fundamental component present in the output voltage is 5961V and the THD is 26.60%.

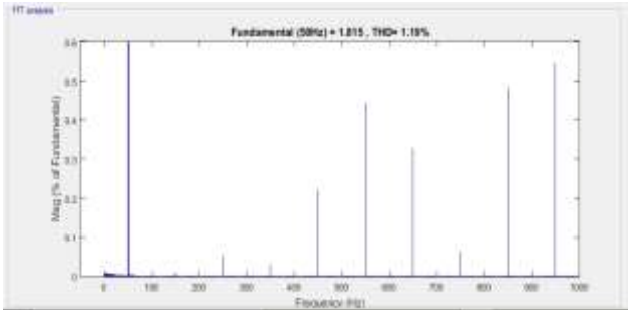

Fig.8. THD Analysis of output current

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It indicates the fundamental component present in the output current is 1.815A and the THD is 1.19%.

4. CONCLUSION

This paper introduces a new multilevel Voltage Source Inverter for medium-voltage applications. This topology is the enhancement of the four-level NNPC converter that is operating over a wide range of input voltage. It has less number of components and the voltage across the power semiconductors is only one-fourth of the dc-link voltage.
SPWM strategy is used in two methods. First method involves comparing sinewave and output levels and the second method involves comparing sinewave and multicarrier triangular signals. These two methods are used to control the output voltage and regulate the voltage of the flying capacitors. And THD analysis using MATLAB/Simulink is performed for both methods. Results indicate that SPWM with the method of comparing a sinewave with multicarrier triangular signal has less harmonic distortions in the output current. The proposed strategy is very intuitive and simple to implement in a digital system.

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