UGC Approved Journal

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 5, Issue 8, August 2017

Design of OFDM Transceiver using Mixed Radix 8-2 Algorithm

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Abstract: Orthogonal Frequency Division Multiplexing (OFDM) is a Frequency Division Multiplexing (FDM) technique used as a digital multi-carrier modulation method. OFDM uses the spectrum efficiently compared to Frequency Division Multiple Access (FDMA) by spacing the channels much closer and creating all the carriers orthogonal to one another. The Existing system, may fail to support high speed efficient data transmission. To improve the speed and maximum amount of data transmission OFDM system may be used. Orthogonality of the carriers prevents interference between the closely spaced carriers and provides high bandwidth efficiency. This work focuses on design and implementation of OFDM transmitter and receiver using the mixed radix8-2 algorithm The design has been coded in VERILOG. Timing simulation is analyzed using Xilinx ISE 13.1.

Keywords: OFDM, IFFT, FFT, ICI.

I. INTRODUCTION

Orthogonal frequency-division multiplexing (OFDM) is a method of digital signal modulation in which a single data stream is split across several separate narrowband channels at different frequencies to reduce interference and crosstalk Orthogonal frequency division multiplexing (OFDM) is a multi-carrier digital modulation technique that has been recognized as an excellent method for high speed bi-directional wireless data communication. OFDM effectively squeezes multiple modulated carriers tightly together, reducing the required bandwidth but keeping the modulated signals orthogonal so they do not interfere with each other. This means symbols sent in the substreams are longer and spaced farther apart. To generate OFDM successfully the relationship between all the carriers must be carefully controlled to maintain the orthogonally of the carriers.

A. Orthogonality Definition

The key to OFDM is maintaining orthogonality of the carriers. If the integral of the product of two signals is zero over a time period, then these two signals are said to be orthogonal to each other. Two sinusoids with frequencies that are integer multiples of a common frequency can satisfy this criterion. Therefore, orthogonality is defined by Eq.(1):

$$\int_0^T \mathrm{Cos}(2\pi n f_0 t)\mathrm{Cos}(2\pi m f_0 t)dt = 0 \ (n \neq m) \qquad \ldots\ldots \text{Eq.(1)}$$

Where n and m are two unequal integers; f_o is the fundamental frequency; T is the period over which the integration is taken. For OFDM, T is one symbol period and fo set to 1/T for optimal effectiveness

The basic idea is to divide a single high rate data stream into a number of lower-rate data streams as shown in to Figure1.1. Each of these data streams is modulated on a specific carrier, which is called subcarrier, and transmitted simultaneously. Such a kind of multi-carrier modulation preserves the robustness against the effects of multipath fading. Moreover, these subcarriers are orthogonal to one another so as to enhance the spectrum efficiency compared to that in conventional multi-carrier transmission. Since the data streams carried by each subcarrier are separated by frequencies, OFDM is also considered as a frequency division multiplexing (FDM) scheme shown in Figure 1.2 for the spectrum of OFDM subcarrier .

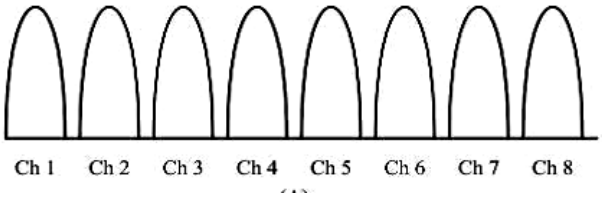

Fig.- 1.1 Spectrum of FDM showing Guard Bands

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Vol. 5, Issue 8, August 2017

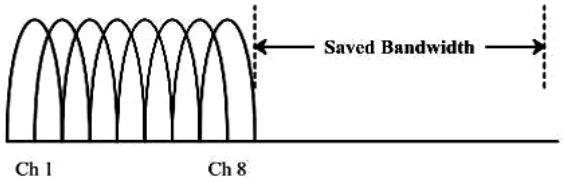

Fig. 1.2 Spectrum of OFDM showing Overlapped Subcarrier

The main reason to use OFDM is to increase the robustness The total signal bandwidth, in a classical parallel data system, can be divided into N non-overlapping frequency sub channels. Each sub-channel is modulated a separate symbol and then N sub-channels are frequency multiplexed. The general practice of avoiding spectral overlap of sub channels was applied to eliminate inter-carrier interference (ICI).This resulted in insufficient utilization of the existing spectrum against the selective fading or narrowband interference.

B. OBJECTIVES

The objective of this developed system is below

- To reduce the complex multiplication and complex addition of FFT and IFFT in proposed work uses the mixed radix 8-2 algorithm.
- To carry an efficient implementation of the OFDM system (i.e. transmitter and receiver) the design and experiments carried on a Xilinx 13.1.

II. BACKGROUND OF OFDM

OFDM is a multi-carrier modulation technique with densely spaced subcarriers that has gained a lot of popularity among the broadband community in the last few years. Orthogonal frequency division Although OFDM has become widely used only recently, the concept dates back some 40 years.

Year	Event
1966	Chang shows that multi-carrier modulation .Can solve the Multipath problem without reducing data rate [10]. This is generally considered the first official publication on multi-carrier modulation. Some earlier work was Holsinger's 1964 MIT dissertation [9] and some of Gallager's early work on water filling [11].
1985	Cimini at Bell Labs identifies many of the key issues in OFDM transmission and does a proof-of-concept design
1993	DSL adopts OFDM, also called discrete multi-tone, following successful field trials / competitions at Bellcore versus equalizer based systems
1999	The IEEE 802.11 committee on wireless LANs releases the 802.11a standard for OFDM operation in 5GHz UNI band
2002	The IEEE 802.16 committee releases an OFDM-based standard for wireless broadband access for metropolitan area networks under revision 802.16a
2003	The IEEE 802.11 committee releases the802.11g standard for operation in the 2.4GHz band.

A. **Research Work**

In 2011, K. Harikrishna and T. Rama Rao proposed Pipeline architecture for Wi-MAX technology using Radix-4 Decimation in frequency FFT algorithm [1]. They used in SEP increases the stability region but reduces the network lifetime and 14 throughput. proposed a memory based recursive FFT design which has much less gate counts, lower power consumption and higher speed. The proposed architecture has three main advantages: fewer butterfly iteration to reduce power consumption, pipeline of radix–2butterfly to speed up clock frequency, and even distribution of memory access to make utilization efficiency in SRAM ports. They coded this design in Verilog hardware description language with increase in speed & performance of OFDM. Ashish D. Sawant et.al [1] proposed the "Study of FPGA Based OFDM Transmitter and Receiver". This proposed section presents relevant works related to OFDM implementation. In his work he used the radix-2 algorithm for designing the OFDM in which they have shown the results for the 64 point FFT and study the performance of OFDM, including the power spectral density, BER. Through intensive MATLAB simulation in this they optimize FFT/IFFT Length was 1024 points and the best value for the SNR was 60db.

A. S. Chavan et.al [2] proposed the work on "FPGA Based Implementation of Baseband OFDM Transceiver Using VHDL" The system is designed using VHDL, synthesized using high level synthesis tool and targeted on Xilinx

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Spartan 3e device.. Resources utilization for transmitter and receiver is given in his paper. DIT radix-2 butterfly approach is used to calculate IFFT and FFT. In their work they only show that the main problem of OFDM transceiver is the processing time which is consumed in the IFFT and FFT.

Manjunath Lakkannavar et.al [3] proposed the work on "Design and implementation of OFDM using VHDL and FPGA". He implemented the OFDM system on FPGA using VHDL it worked for 8-point FFT using radix-2 algorithm. In 2010,Mounir Arioua et. al. [2] proposed an optimized implementation of 8- point FFT processor with radix-2 algorithm in R2MDC architecture. The main issue in FFT operation is the complex multiplication so, they tried to reduce the complexity one of two proposed methods replaces the expensive complex multiplication. For this they have applied the methods to 8-point FFT and compared it to conventional FFT and R2MDC processor. They designed 8-point FFT with radix-2 in R2MDC architectures and was first coded in VHDL. Then they have proposed a novel 8-point FFT processor based on pipeline architecture with no complex multiplication and compared to Cooley-Tukey and R2MDC processor

III. SYSTEM DEVELOPMENT

Wireless communication using OFDM has many advantages. Channel equalization using OFDM is easy as compare to adaptive equalization. Also spectrum available can be used more efficiently with help of OFDM. Applications such as DAB, HDTV, Wireless LAN (IEEE 802.11a, g) where high baud rate & less noise are essential features, OFDM can be efficiently used. FPGAs can used to implement the hardware of any system at very less cost.

A. PROPOSED SYSTEM

The proposed work is to design the 48-point FFT & IFFT blocks for OFDM by using mixed radix8-2 algorithm and to achieve the efficient multiplication. The design is coded in Verilog and synthesis is done in Xilinx ISE 13.1 software The main problem in OFDM is to minimize the processing time and power consumption of OFDM system. The mixed radix 8-2 algorithm is to solve the FFT and IFFT it can be reduce the processing time in OFDM system. Initially transmitter and receiver is implemented independently and tested Xilinx 13.1 Then both the subsystems were merged to form one system. Design flow for both the system is same. Then the algorithm is developed for the sequential and concurrent operations. To make the design more parallel the operations are broken in to processes and independently written in VHDL. Some blocks contain floating point complex operations, for that Intellectual Property (IP) cores provided by Xilinx are used. The control server is externally powered. The hardware description is developed using Verilog and synthesized using Xilinx 13.1

B. OFDM TRANSMITTER DESIGN

The main components of OFDM transmitter are shown in Fig.3.3. The randomizer is used as random bit generator the first three blocks are used for data coding and interleaving. The coded bits will be mapped by the constellation modulator using QPSK, this way an + jbn values are obtained in the constellation of the modulator. The serial to parallel converter converts the data bits from the serial form to the parallel form. The Inverse Fast Fourier Transform (IFFT) transforms the signals from the frequency domain to the time domain; an IFFT converts a number of complex data points, of length that is power of 2, into the same number of points but in the time domain.

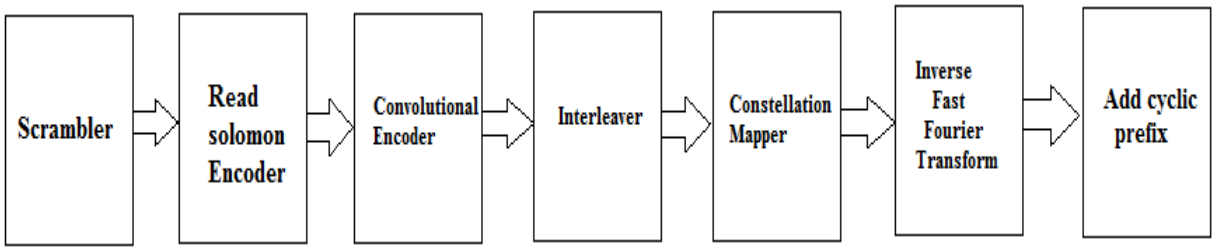

Figure 3.3 Block Diagram of OFDM Transmitter Design

Specification are listed below
- All the sub-carriers are modulated using QPSK
- IFFT: 48-point. Implemented using FFT Mixed Radix 8-2 algorithm
- Channel coding: Reed Solomon code + Convolutional code
- Reed Solomon Encoder: RS (15, 9)
- Convolutional Encoder: m=1, n=2, k=7. Code rate = ½
- Block Interleaver and 1/8 Cyclic Prefix

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C. OFDM RECEIVER DESIGN

The OFDM receiving unit receives its input directly from the transmitter whenever its output is available. The receiver follows an exact reverse procedure of which was followed in the transmitter. It receives the complex (modulated) output points and performs demodulation and recovers the original bits sent to the transmitter. The received symbol is in time domain and it is distorted due to the effect of the channel. The received signal goes through a serial to parallel converter and cyclic prefix removal. After the cyclic prefix removal, the signals are passed through an N-point fast Fourier transform to convert the signal to frequency domain. The output of the FFT is formed from the first M samples of the output. The work of the project is focused on the design and implementation of FFT for FPGA kit. The direct mathematical derivation method is used for this design.

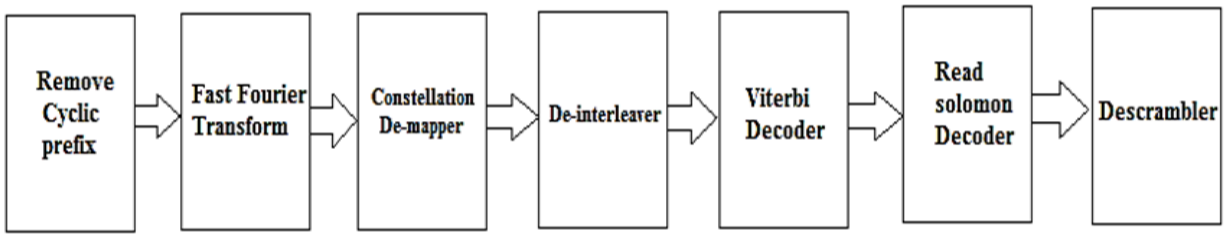

Figure 3.4 Block Diagram of OFDM Receiver Design

The main blocks of OFDM receiver are observed in Figure 3.4 the received signal goes through the cyclic prefix removal and a serial-to-parallel converter [2]. After that, the signals are passed through an N-point fast Fourier transform to convert the signal to frequency domain. The output of the FFT is formed from the first M samples of the output The demodulation can be made by DFT, or better, by FFT, that is it efficient implementation that can be used reducing the time of processing and the used hardware. FFT calculates DFT with a great reduction in the amount of operations, leaving several existent redundancies in the direct calculation of DFT [4].

IV. PERFORMANCE ANALYSIS

A. EXPERIMENTAL ANALYSIS FOR OFDM TRANSMITTER AND RECEIVER

Experimental analysis deals with development of system on software and hardware platform. The developed system is coded in Verilog HDL. It is synthesized and simulated on Virtex7 XC7V2000T based device using Xilinx Foundation ISA Environment 13.1 and Modalism's-XE. Technology view describes top block which shows the set of inputs and outputs. Register Transfer Logic (RTL) view designates the internal architectural blocks along with the connections between input and output pins.

I. RTL SCHEMATIC FOR OFDM TRANSMITTER

The RTL Viewer allows viewing schematic representations of the internal structure of the designs . Register Transfer Level (RTL) is a design abstraction which models a synchronous digital circuit in terms of digital signals (data) between hardware registers and the logical operations performed on those signals. RTL is shown in Figure 4.1. It represents black box of top level entity of the transmitter.

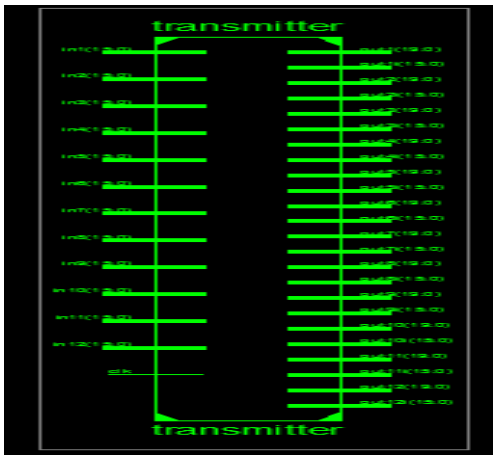

Figure 4.1 RTL Schematic for Transmitter Module

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Figure 4.2 represents the RTL schematics for each block inside the transmitter which are interconnected to each other. The input for each transmitter is 12 data point and output which is transmitted is 12 complex data point.

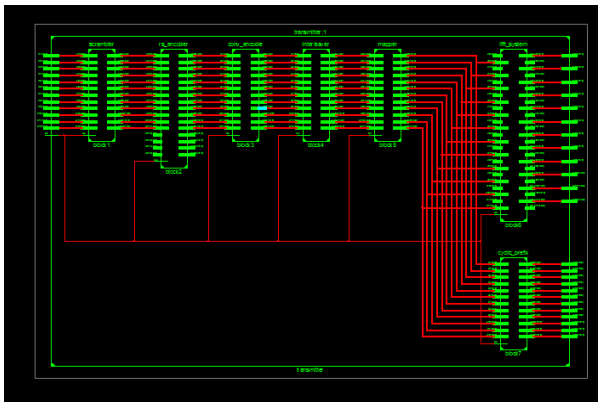

Figure 4.2 RTL Schematics for Blocks Inside Transmitter

II. RESOURCE UTILIZATION FOR OFDM TRANSMITTER

Resource utilization for implementation of complete OFDM Transceiver using mixed radix 8-2 is enlisted in Table 4.1 Based on the percentage of resources consumed it is quite possible to estimate the area of the design. It also expresses the complexity of the design.

Table 4.1 Resource Utilization for OFDM Transmitter

Parameter	Used	Available	Utilization (%)
Number of Slice Resister	2644	2443200	0
Number of Slice LUT	4699	1221600	0
Number of Fully Used LUT FFPair	2153	5190	41
Number of Bound IOBs	625	1200	52
Number ofBUFG/BUFGCTRLs	1	128	0
Number of DSP48E1s	95	2160	4

According to the resource utilization summary for OFDM transmitter which is given after the synthesis of the program. Figure 4.3 shows chart for the percentage of the resource utilization for the complete OFDM Transceiver proposed system.

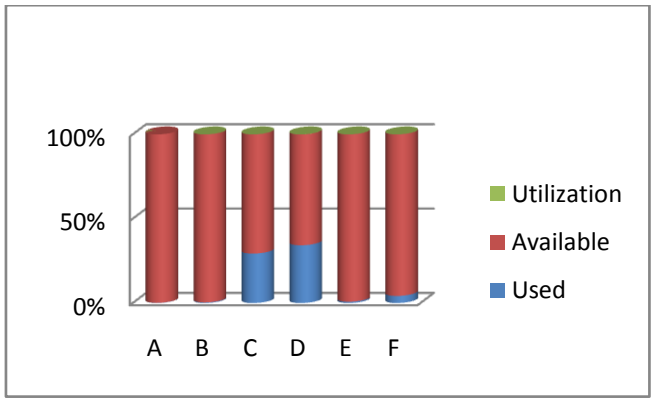

Figure 4.3 Resource Utilization Chart for OFDM Transmitter

III.RTL SCHEMATIC FOR OFDM RECEIVER

The Figure 4.4 represents RTL schematic generated in synthesis for OFDM Receiver. It represents black box of top level entity of receiver.

The RTL schematics for each block inside the receiver which are interconnected to each other shown in Figure 4.5. The input for each receiver is 12 complex data point and output which is received is 12 data point after decoding.

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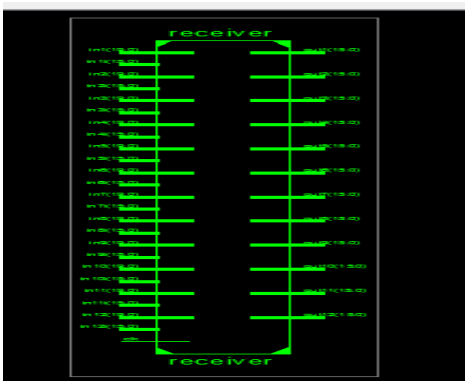

Figure 4.4 RTL Schematic for Receiver Module

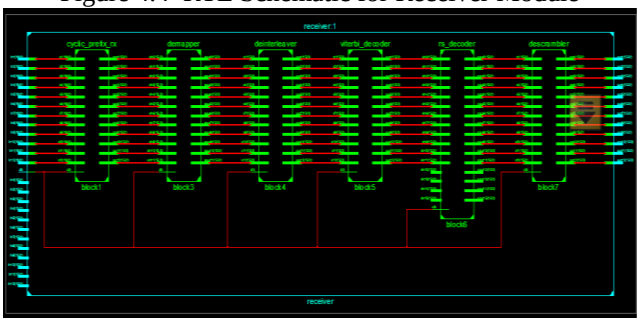
Figure 4.5 RTL View for Inside Block of Receiver

IV. RESOURCE UTILIZATION FOR OFDM RECEIVER

Resource utilization for implementation of complete OFDM receiver using mixed radix 8-2 is enlisted in Table 4.2. Based on the percentage of resources consumed it is quite possible to estimate the area of the design. It also expresses the complexity of the proposed system design.

Table 4.2 Resource Utilization for OFDM Receiver

Parameter	Used	Available	Utilization (%)
Number of Slice Resister	2644	2443200	0
Number of Slice LUT	4699	1221600	0
Number of Fully Used LUT FF Pair	2153	5190	41
Number of Bound IOBs	625	1200	52
Number of BUFG/BUFGCTRLs	1	128	0
Number of DSP48E1s	95	2160	4

According to the resource utilization summary for OFDM Receiver which is given after the synthesis of the program. From the Figure 4.6 we says that the chart shows the percentage of the resource utilization for the complete OFDM receiver.

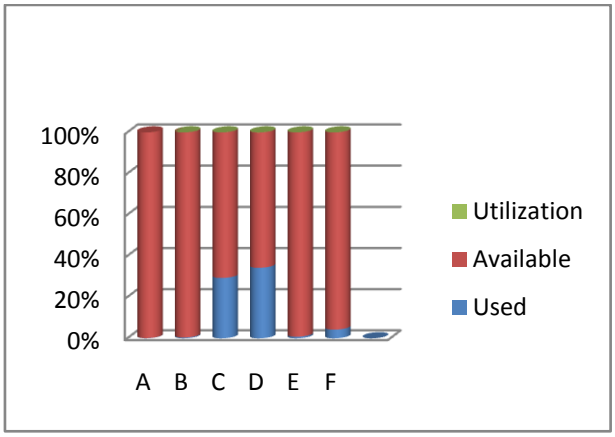

Figure 4.6 Resource Utilization Chart for OFDM Receiver

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4.3.1 Simulation for OFDM Transmitter

After the simulation of the OFDM transmitter the test bench waveform are generated. The developed system for the transmitter has timing waveform for transmitted 12 data inputs shown in Figure 4.7.

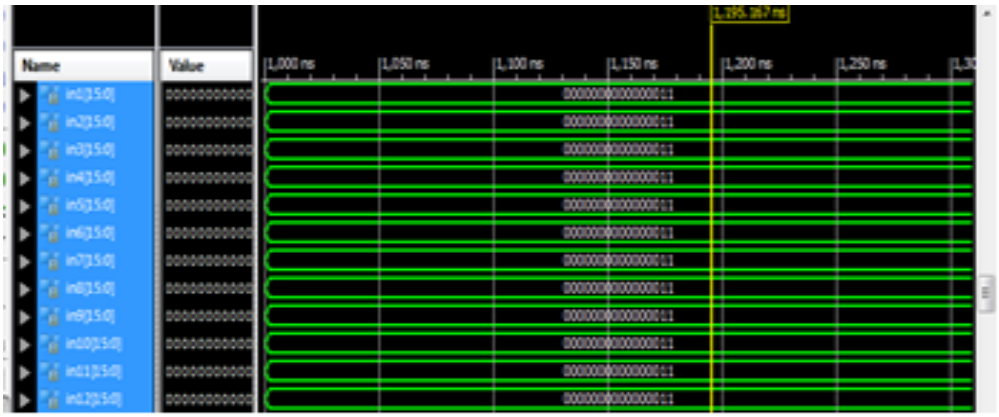

Figure 4.7 Timing Waveform of Inputs for Transmitter

Figure 4.11 represents the timing waveform of output for transmitter which are transmitted after encoding having the 12 complex data point.

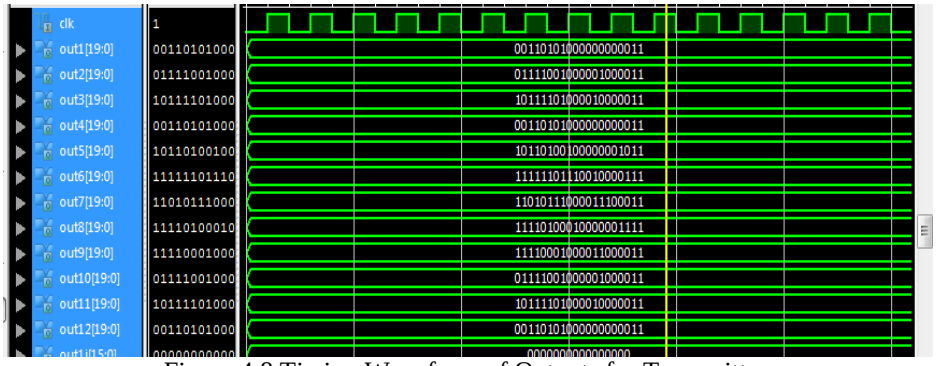

Figure 4.8 Timing Waveform of Outputs for Transmitter

4.3.2 Simulation for OFDM Receiver

After the simulation of the OFDM receiver, the test bench waveform are generated .In the developed system for the receiver has 12 complex data inputs received from transmitter are shown in Figure 4.12. Similarly, in such way those remaining 36 data points are received.

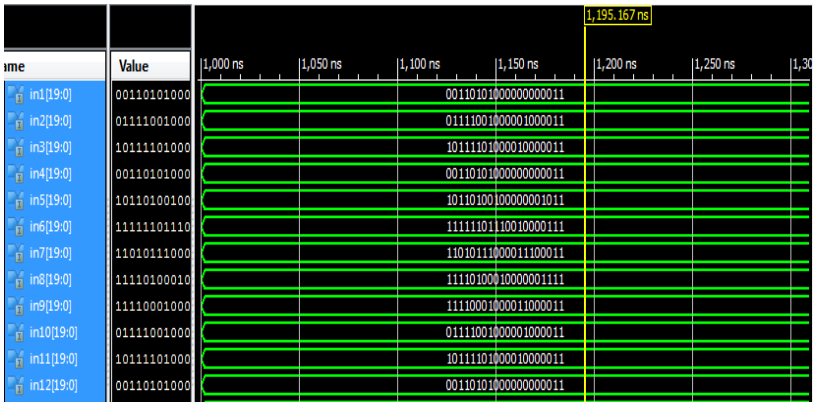

Figure 4.9 Timing Waveform of Inputs for Receiver

Figure 4.10 represents the timing waveform of output for receiver has the 12 data point for first receiver .Similarly, in such way that remaining 36 data point are received.

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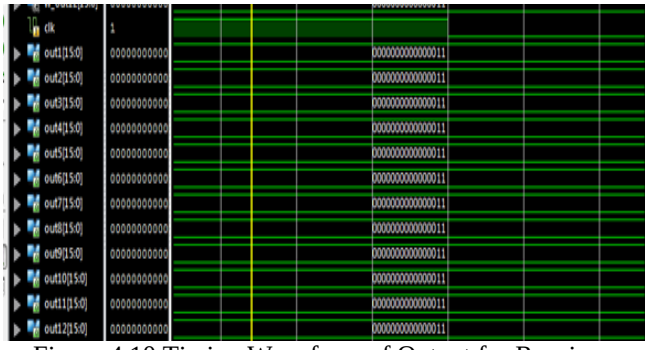

Figure 4.10 Timing Waveform of Output for Receiver

V. RESULT

For proposed system by using the Mixed Radix8-2 algorithm in OFDM transmitter and receiver minimize the transmitter and receiver processing time up to **6.450ns.** For proposed system, there are some parameter for transmitter and receiver. Table 4.3 represents comparative analysis of transmitter and receiver obtained result

Table 4.3 Represents Comparative Analysis of Transmitter and Receiver

Parameter	**Transmitter**	**Receiver**
Number of Slice Resistor	2644/2443200	2644/2443200
Number of LUTs	4699/1221600	4699/1221600
Minimum Period(nS)	6.45	6.450
Maximum Frequency(MHz)	155.038	155.038
Throughput(Gbps)	119.06	119.06
Memory Usage(Kb)	40777	446240

VI. CONCLUSION

In this project work, the design of an OFDM transmitter and receiver is modified with mixed radix algorithms and that are implemented using VLSI design process. It was found during the algorithm design that many blocks need complex multipliers and adders and therefore special attention needs to be given to optimize these circuits and maximize reusability The developed system, has given the 48 data point is transmitted by the transmitter and at the receiver end receive the same data without any loss in the minimum time. In all previous work, if compare the delay time for that system required more than this proposed system

It is found that, this architecture of the FFT processor is efficient for transmission of data at high speed. Hence it is very much useful for the OFDM system. The device used is Vertex-7 using Xilinx ISE 13.1 software. The delay time found in this project is 6.450 nS. Hence the proposed FFT processor is efficient.

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