IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

International Journal of Innovative Research in
Electrical, Electronics, Instrumentation and Control Engineering

ISO 3297:2007 Certified

Vol. 4, Issue 9, September 2016

Phase Shifted Semi Bridgeless AC DC Converter

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Abstract: A Plug in hybrid electric vehicle is a hybrid vehicle with a storage system that can be recharged by connecting a plug to an external electric power source. The charging ac outlet inevitably needs an onboard ac dc charger with power factor correction. The two stage approach with cascaded PFC ac–dc and dc–dc converters is the common architecture of choice for PHEV battery chargers, where the power rating is relatively high, and lithium ion batteries are used as the main energy storage system. In the two stage architecture, the PFC stage rectifies the input ac voltage and transfers it into a regulated intermediate dc link bus. At the same time, PFC is achieved. Phase shifted semi bridgeless ac dc converter is proposed to simplify the current sensing technique for semi bridgeless PFC converter. The converter features high efficiency at light loads and low ac input lines, which is critical to minimize the charger size, charging time, and amount and cost of electricity drawn from the utility. The converter is ideally suited for residential charging applications.

Keywords: AC–DC power converters, boost converter, bridgeless power factor correction (PFC), current sensing, plug-in hybrid electric vehicle (PHEV) charger.

I. INTRODUCTION

A Plug in hybrid electric vehicle is a hybrid vehicle with a storage system that can be recharged by connecting a plug to an external electric power source. The charging ac outlet inevitably needs an onboard ac dc charger with power factor correction. A variety of circuit topologies and control methods has been developed for PHEV battery chargers. The two stage approach with cascaded PFC ac–dc and dc–dc converters is the common architecture of choice for PHEV battery chargers, where the power rating is relatively high, and lithium ion batteries are used as the main energy storage system. The single stage approach is generally only suitable for lead acid batteries due to a large low frequency ripple in the output current.

In the two stage architecture, the PFC stage rectifies the input ac voltage and transfers it into a regulated intermediate dc link bus. At the same time, PFC is achieved. A boost derived PFC topology operated in continuous conduction mode is used here as the main candidate for the front end ac–dc PFC converter for PHEV battery charging. The front end candidate topologies in the boost derived class includes the, interleaved boost converter, the bridgeless boost converter, the dual boost converter, the semi bridgeless boost converter, and the proposed phase shifted semi bridgeless (PSSB) boost converter. The converter features high efficiency at light loads and low ac input lines, which is critical to minimize the charger size, charging time, and amount and cost of electricity drawn from the utility. The converter is ideally suited for residential charging applications. The benefits that can be achieved by applying the correct power factor correction are, reduction of power consumption due to improved energy efficiency, reduced power consumption, less greenhouse gas emissions and fossil fuel depletion by power stations. The other benefits are extended equipment life and reduced electrical burden on cables and electrical components.

II. PROPOSED PHASE SHIFTED SEMI BRIDGELESS CONVERTER

The PSSB topology shown in figure 2.1 is proposed as a solution to simplify current sensing in bridgeless PFC boost applications using the current synthesizer sensing method. The inductor current synthesizer technique is used to predict the boost inductor current by sensing the MOSFET current. The proposed topology power train incorporates the decoupled MOSFET gates, similar to that of the dual boost, and uses two slow diodes (Da and Db), similar to that of the semi bridgeless boost, to link the ground of the PFC to the input line. The gating signals for the MOSFETs are 180' out of phase, as shown in Figure 2.1. The phase shifted gating enables the usage of the advanced current synthesizing method, which cannot be used in either the bridgeless topology or the dual boost topology because all controllers available for these topologies require full input current shape sensing.

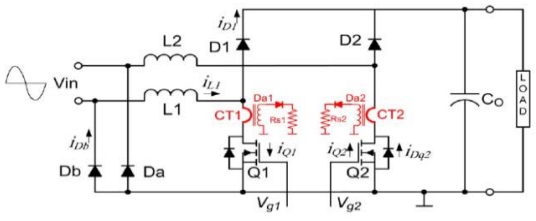

Fig 2.1. Proposed phase shifted AC-DC converter

DOI 10.17148/IJIREEICE.2016.4928

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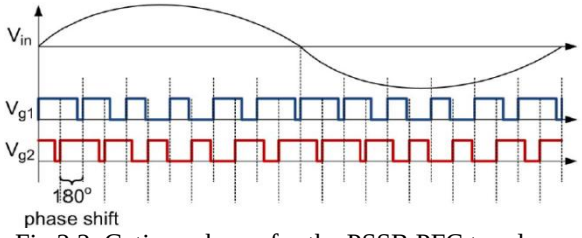

Fig 2.2. Gating scheme for the PSSB PFC topology

III.OPERATIONAL PRINCIPLE

To analyze the circuit operation, the input line cycle is separated into positive and negative half-cycles

A. Positive Half-Cycle Operation

Referring to Fig 2.1, during the positive half-cycle, when the ac input voltage is positive, Q1 turns on and current flows through L1 and Q1 and continues through Q2 and then L2, returning to the line while storing energy in L1 and L2. When Q1 turns off, the energy stored in L1 and L2 is released as current flows through D1, through the load, and returns through the body diode of Q2/partially through Db back to the input

B. Negative Half-Cycle Operation

Referring to Fig.2.1 , during the negative half-cycle, when the ac input voltage is negative, Q2 turns on and current flows through L2 and Q2 and continues through Q1 and then L1, returning to the line while storing energy in L2 and L1. When Q2 turns off, the energy stored in L2 and L1 is released as current flows through D2, through the load, and returns split between the body diode of Q1 and Da back to the input

C Detailed Positive Half Cycle Operation and Analysis for D>0.5

Interval 1: At t_0, Q1 and Q2 are on, as shown in figure 3.1. During this interval, the current in series inductances L_1 and L_2 increases linearly and stores the energy in these inductors. The energy stored in Co provides energy to the load. The return current is split among D_b, Dq_2, and Q2.

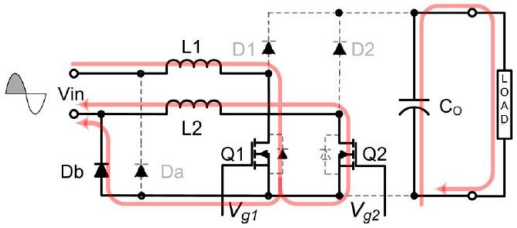

Fig.3.1. Intervals 1and 3: Q1 and Q2 on

Interval 2: At t_1, Q1 is on, and Q2 is off, as shown in Figure 3.2. During this interval, the current in series inductances L_1 and L_2 continues to increase linearly and store the energy in these inductors. The energy stored in Co provides the load energy. The return current is split only between Db and Dq2.

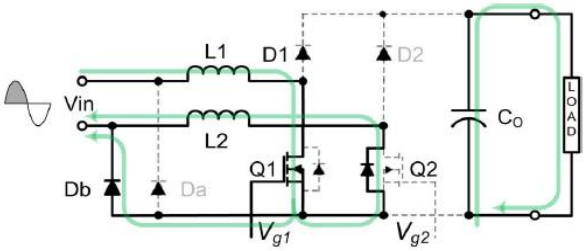

Fig.3.2 Interval 2: Q1 on body diode of Q2 conducting

Interval 3:

At t_2, Q1 and Q2 are on again, and interval 1 is repeated, as shown in Figure 3.1. During this interval, the current in series inductances L_1 and L_2 increases linearly and stores the energy in these inductors. The return current is again split among Db, Dq2, and Q2.

Interval 4:

At t_3, Q1 is off, and Q2 is on, as shown in Figure 3.3. During this interval, the energy stored in L_1 and L_2 is released to the output through L_1, D_1, partially Q2, Dq2, L2, and Db.

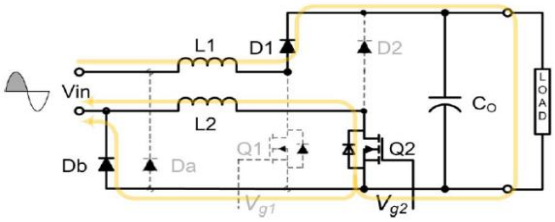

Fig.3.3. Interval 4: Q1 off and Q2 on

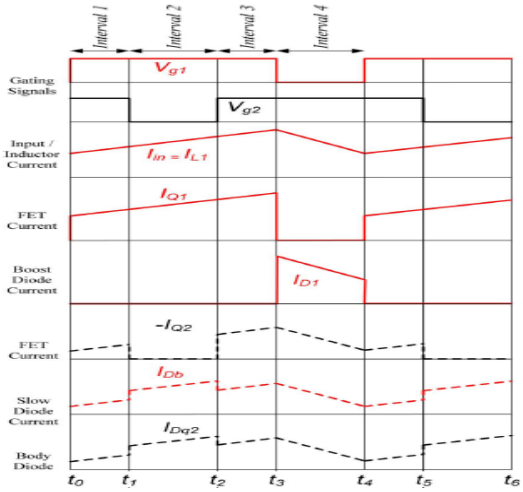

Fig.3.4. PSSB boost converter steady-state waveforms for D > 0.5

IV. SIMULATION ANALYSIS AND RESULT

The proposed converter is simulated and output waveforms are obtained. The converter input voltage is 200 V and output obtained is 400V.

The simulation analysis of the proposed converter is is carried out on the basis of the following assumptions:

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1) Input voltage (V_{in}) = 200V
2) Output voltage (V_o)= 400V
3) Switching frequency(f_s) = 50KHz
4) Duty ratio(D) =53%

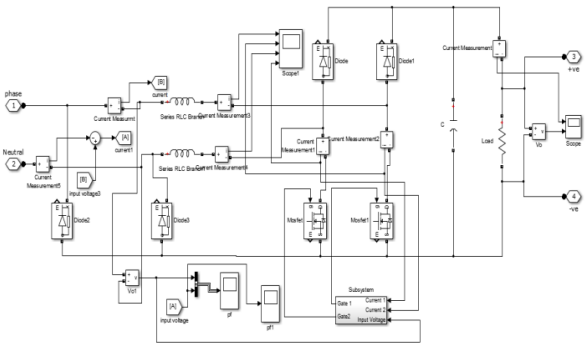

Fig.4.1. closed loop simulation diagram for PSSB converter

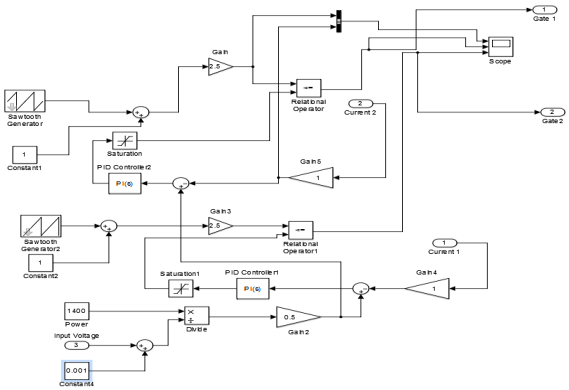

Fig.4.2. Sub system simulation diagram PSSB converter

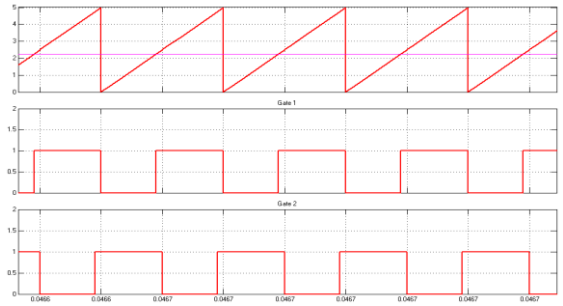

Fig.4.3. Generation of gate pulse in closed loop simulation

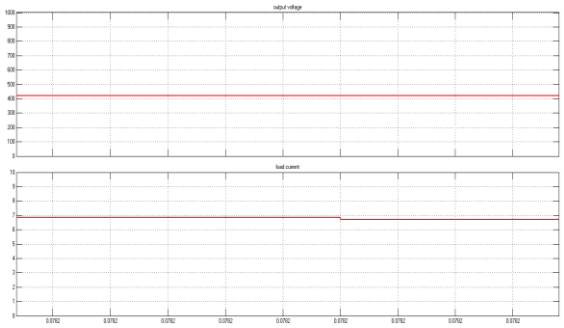

Fig.4.4. output voltage and load current

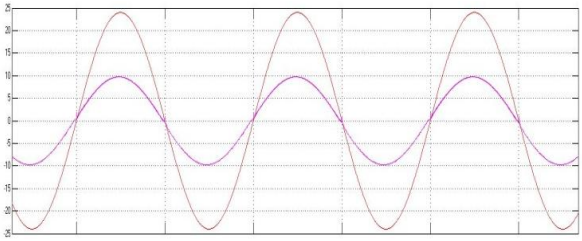

Fig.4.7. input current and input voltage in same phase

V.CONCLUSION

A high performance phase shifted semi bridgeless boost ac–dc boost PFC converter topology has been proposed to simplify the current sensing technique for the semi bridgeless PFC converter. The converter features high efficiency at light load and low line conditions, which is critical to minimize the charger size, cost, charging time, and amount and cost of electricity drawn from the utility. It provides higher efficiency at high power levels and solves the problem of heat management in the input rectifier diode bridge. Conduction losses are minimized due to the presence of only two semiconductor switches in any given conduction path. This converter is less bulky in comparison to the conventional topologies. The closed loop simulation and hardware prototype of the converter is done.

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