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Design and Implementation of ALU Using FinFETs: A Review

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Abstract: An Arithmetic logic Unit (ALU) is the heart of all microprocessors. It performs logical or arithmetic operations. The principal limitations in scaling the bulk CMOS are short channel effects, sub-threshold leakage and gate-dielectric leakage. FinFET has an excellent control on short channel effects within the sub-micron regime as a result growing the probability to scale down the transistor. In this paper, an 8-bit ALU that performs basic logical and arithmetic operations has been designed using FinFET structures and leakage power has been studied and compared with MOSFET structure. The simulation is carried out using TANNER EDA tools.

Keywords: FINFET, Leakage Power, Back Biasing, Independent gate circuit.

I. INTRODUCTION

An Arithmetic Logic Unit (ALU) performs logical or arithmetic operations. It is getting smaller and more complex nowadays to enable the development of a more powerful but smaller computer. However, there are a few limiting factors that slows down the development of smaller and more complex chip when CMOS is used. The primary obstacles in scaling the bulk CMOS are short channel effects, sub-threshold leakage and gate-dielectric leakage. In the design of circuits like ALU fabricated with nanometer CMOS technologies, the handling of power consumption and, in particular, the tradeoff between leakage power and dynamic performance is a challenge. The strategies to tackle this issue involve all the abstraction levels of the design. From the viewpoint of the electron devices, multi-gate FETs realized in a thin silicon film offer good electrical characteristics and an attractive biasing flexibility.

FinFET has a very good control on short channel effects in the sub-micron regime thus increasing the possibility to scale down the transistor. Due to this reason, the small length transistor can have a larger intrinsic gain and a very less off-state current compared to the bulk counterpart. Drain to source capacitance is very less which leads to reduction in power consumed. In addition, there is no "reverse body effect" in these transistor devices. It has an improved latch-up, noise, and current immunity through the substrate.

In fact, the FinFET technology can fabricate transistors with either a single gate surrounding the silicon fin [three-terminal (3T), Fig. 1(a)], or two gates which can be independently biased [four-terminal (4T), Fig. 1(b)] . The 3T FinFETs or the planar double- gate MOS (DGMOS) transistors with a very thin silicon film has a better sub-threshold slope and drain induced barrier lowering (DIBL) with respect to conventional bulk MOSFETs, thus reducing the sub-threshold leakage. Furthermore, FinFETs with independent gate have the superiority in threshold-voltage (VT) and leakage-current control.

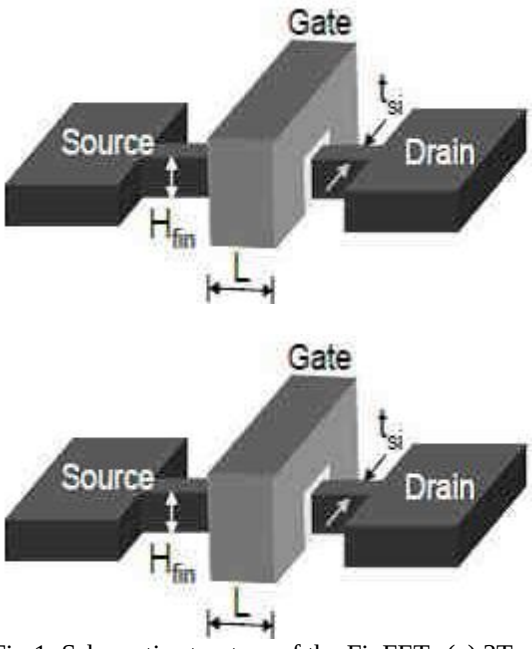

Fig 1: Schematic structure of the FinFETs (a) 3T FinFET. (b) 4T FinFET

From a circuit perspective, the reduction of the leakage current can be pursued by using stacked transistors and by changing the threshold voltage through back biasing, i.e., the body terminal for the bulk MOSFETs or the back-gate terminal for the FinFETs is biased at a non-zero voltage in both cases at the cost of an increase of the delay.

These circuit techniques can potentially benefit a lot from the biasing flexibility offered by FinFETs with independent gates, thus giving to FinFETs a significant edge over conventional bulk MOSFETs.

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A. ARITHMETIC LOGIC UNIT

Methodology:

In order to design the Arithmetic Logic Unit, the following procedures have been used as a general guideline.

1. State the specification of the desired functions of ALU by using truth table and any other means wherever possible.
2. Minimize or transform it to the desired logic gates like XOR, XNOR, and so on.
3. Draw the schematic for the logic diagram using S-edit and compile the schematic
4. The design is implemented in transistor level.
5. The performance of ALU is obtained through H-Spice or TANNER EDA tools.

The design of 8-bit arithmetic unit as shown in Fig:3 performs two arithmetic, seven logical operations l.8-bit ALU is designed by cascading eight 1-bit ALU blocks. There is a 2:1 multiplexer in the end to choose between arithmetic or shifting/rotating operations.

Each 1-bit ALU is composed of the following four components:

l. 2:1 multiplexer to decide add/sub operation
2. Circuit that does add and subtract
3. Logical 8:1 multiplexer

The block diagram of the 1 bit arithmetic unit is shown in Fig 2. The operation of the 8 bit ALU is depicted in the truth table as shown in Table 1.

Sel2	Sel1	Sel0	function
0	0	0	ADD/SUB
0	0	1	NOT
0	1	0	AND
0	1	1	NAND
1	0	0	OR
1	0	1	NOR
1	1	0	EXOR
1	1	1	EXNOR

Table I: Operations of ALU

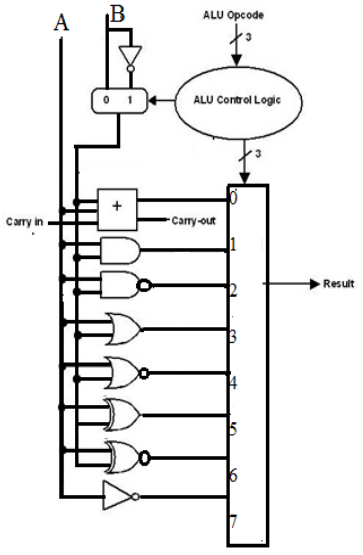

Fig 2: One Bit Arithmetic Logic Unit

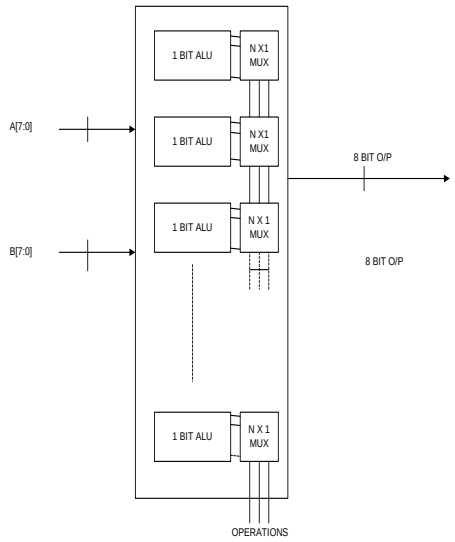

Fig3: Block diagram of 8 bit arithmetic unit

II. LITERATURE SURVEY

Literature survey is an important part of the review paper. It enables assimilation of knowledge required for the project right from the problem definition, finding a solution for the same and its execution. The following section summarizes the literature survey carried out for the paper.

S. Jim Hawkinson presented a paper entitled as "Analysis and Perfirmence Comparison of CMOS and FINFET for VLSI applications" [1]. In this, investigation resulted the basic gates and memory circuits like 6T SRAM are modeled in HSPICE software using CMOS structure and FinFET structures are analyzed and their performances like standby power Consumption and static noise margin are compared. Also a low power and robust 6T SRAM cells based on FinFET has been proposed.

Aqilah binti Abdul Tahrim, Huei Chaeng Chin, Cheng Siong Lim, andMichael Loong Peng Tan, presented " Design and Performance Analysis of 1-Bit FinFET Full Adder Cells for Sub threshold Region at 16 nm Process Technology". In this work, the FinFET structure is implemented in 1-bit full adder transistors to investigate its performance and energy efficiency in the subthreshold region for cell designs of Complementary MOS (CMOS), Complementary Pass-Transistor Logic (CPL), Transmission Gate (TG), and Hybrid CMOS (HCMOS).

The performance of 1-bit FinFET-based full adder in 16-nm technology is benchmarked against conventional MOSFET-based full adder. Propagation delay, average power dissipation, power-delay-product (PDP), and energy-delay-product (EDP) are analysed based on all four types of full adder cell designs of both FETs. The 1-bit FinFET-based full adder shows a great reduction in all four metric performances. A reduction in propagation delay, PDP, and EDP is evident in the 1-bit FinFET-based full adder of CPL, giving the best overall performance due to its high-speed performance and good current driving capabilities[2].

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Anthony Chand designed cost affective ALU , The paper entitled as" Cost affective ALU designs that save energy with increased performance" [3] .The purpose of this paper was to read to and review different design for ALU's and to find one that had an increased throughput while saving energy and being cost effective so is can also be implemented easily. One ALU architectures that seem to be idea for the purpose of this review be the CPL design with a dual power supply because it has performance increase and it cost effective with energy saving. the implantation of a QCA full adder will make the ALU design complexity decease while have solving issues that are present in the current CMOS technology.

The paper entitled as "**Design And Analysis Of Finfet Based High Performance 1-Bit Half Adder-Half Subtractor Cell"**[4], presented by Ruchi dantre, Sudha yadav Double gate FinFETs are emerging transistors, which gives better short channel effects performance compared to conventional MOSFET transistors .Adders and sub-tractors are very basic components in computation. Most of the operations such as multiplication, division, ripple carry addition etc. require Adder and sub-tractor as a basic building block. The efficiency of any system depends on the performance of internal components. If internal components satisfy the criteria of area, power and delay, the system will always be a efficient system.

Jency Rubia J, Gopal B.G, Prabhu V designed 4-Bit Full Adder using FinFET. To replace nano scale CMOS, a multi gate device called FinFET is proposed. FinFET has its own advantages over the CMOS such as reduction in leakage power, operating power, leakage current and transistor gate delay, reduced threshold level and steeper sub threshold swing. The target of this paper is to reduce and calculate leakage power of 4-Bit full adder using FinFET. [5].

Michael C. Wang gives the idea about Independent-Gate FinFET Circuit Design Methodology. Usually, the second gate of FinFETs is used to dynamically control the threshold voltage of the first gate in order to improve circuit performance and reduce leakage power. However, we can also utilize the second gate to implement circuits with fewer transistors. This is important since area efficiency is one of the main concerns in modern circuit design. In this paper, a methodology for effectively synthesizing logic circuits using both gates of FinFETs as inputs is presented. Simulation results show that independent-gate FinFET circuit implementation has significant advantages over single-gate FinFET circuit implementation in terms of power consumption and cell area. [6].

Ajay N. Bhoj, Niraj K. Jha presented **"Design of Logic Gates and Flip-Flops in High-Performance FinFET Technology"** In this paper, for the first time, They evaluate symmetric (Symm-Φ_G) and asymmetric (Asymm-Φ_G) gate-work function FinFETs head to head in a high-performance process, using technology computer-aided design 3-D device simulations. They demonstrate that Asymm-Φ_G shorted-gate (a-SG) n/p-FinFETs, which use both workfunctions corresponding to typical high-performance metal-gate n/p-FinFET1s, are promising, as they can yield over two orders of magnitude lower leakage without excessive degradation in ON-state current, in comparison to Symm- ΦG shorted-gate (SG**)** FinFETs, placing them in a better position **than** back-gate biased independent-gate (IG) FinFETs for leakage reduction. Thereafter, we explore the design space of FinFET logic gates, latches, and flip-flops, for optimal tradeoffs in leakage versus delay and temperature, using mixed-mode 2-D device simulations. Elementary logic gates (such as INV, NAND2, NOR2, XOR2, and XNOR2) using Asymm-Φ_G SG-mode FinFETs appear to be located optimally in the leakage-delay spectrum, in comparison to the most versatile configurations possible by mixing corresponding Symm-Φ_G SG- and IG-mode FinFETs. Latches and flip-flops, however, require an astute combination of Symm-Φ_G and Asymm-Φ_G FinFETs to optimize leakage, delay, and setup time simultaneously.[7].

Raj Lakshmi Shukla , Rajesh Mehra presented "Design Analysis and Simulation of 1 bit Arithmetic Logic Unit on different foundaries". In this paper an ALU has been designed and implemented using different foundaries like 45nm, 65nm and 90 nm. The performance of developed ALU has been analyzed and compared in terms of area and power using BSIM4 device model. The schematic of ALU circuit has been designed using DSCH 3.5 and its equivalent layout has been created using Microwind tool. It can be observed from simulation results that 45nm technology based ALU has shown area reduction ranging from 48 % to 75% with 65nm and 90nm technology and power reduction from 84% to 97.9% as compared with 65nm and 90nm based technologies [8].

The paper entitled as "**Design and Implementation of Area Optimized ALU using GDI Technique**" presented by **Akshay Dhenge, Abhilash Kapse, Sandeep Kakde .** The purpose of this paper is the design and implementation of anArithmetic Logic Unit (ALU) using area optimizing techniques such as complementary & Gate-Diffusion-input (GDI). The main sub-blocks of ALU are Adder, Subtractor, shifter and Logical Block. This work evaluates and compares the performance and optimized area of ALU with Static CMOS technique and GDI technique in 250nm CMOS (1P5M-1 Poly 5 Metal) process technology. Simulat ions are performed by using Tanner EDA 13.2 tools using model file 250nm CMOS technology. At first, using Tanner 13.2 EDA S-Edit Tool, the circuits are implemented with Static CMOS technology and then with GDI techniques. Simulations results validate the proposed concept and verify that GDI technique decreases the area used by ALU and increase the speed of ALU [9].

Prateek Mishra, Anish Muttreja, and Niraj K. Jha gives the idea about FinFET Circuit Design . The two gates of a FinFET can either be shorted for higher perfomance or independently controlled for lower leakage or reduced transistor count. This gives rise to a rich design

space. This chapter provides an introduction to various interesting FinFET logic design styles, novel circuit designs, and layout considerations. [10].

III. APPLICATIONS

1) Sameer Dwivedi, Dr. Neelam Rup Prakash N gives Advancements in VLSI Technology using FinFETs .scaling up to sub-micron region, single-gate MOSFETs has served the purpose but as designing moves down in ultra sub-micro region, the further scaling of single gate MOSFETs leads to a number of Short Channel Effects which directly affects the various performance criteria and to resolve these effects, Multi-gate MOSFETs are designed and one of the most widely used and efficient is FinFET.[11].

2) Girish H, Shashi Kumar D. R presents a survey on the performance analysis of FinFET SRAM Cells for different technologies.Industry requires high performance low power devices and memories. FinFET has become the most promising alternatives to conventional CMOS. In this paper, comparison of conventional CMOS, Independent-Gate (IG) and Tied Gate (TG) FinFET SRAM standard cells performance analysis is done with respect to leakage power, Static Noise Margin (SNM) and delay.[12]

IV. CONCLUSION

This paper provides the design and different implementation of VLSI Technology using FinFETs and their performance. In the proposed method an 8-bit ALU is designed using MOSFET and FinFET. It performs a total of 24 operations of which one is arithmetic, 7 are logical operations. The simulation will be carried out using TANNER EDA tools. Power and Delay analysis is major area of concern.

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