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Innovative Approach of Designing Multilevel Inverter with Reduced Number of Switches

Sangita Das Biswas[1], Moumita Saha[2], Priyanka Debbarma[3]

Asstt. Professor, Dept. of Electrical Engineering, Tripura University (A Central University), Agartala, India[1]

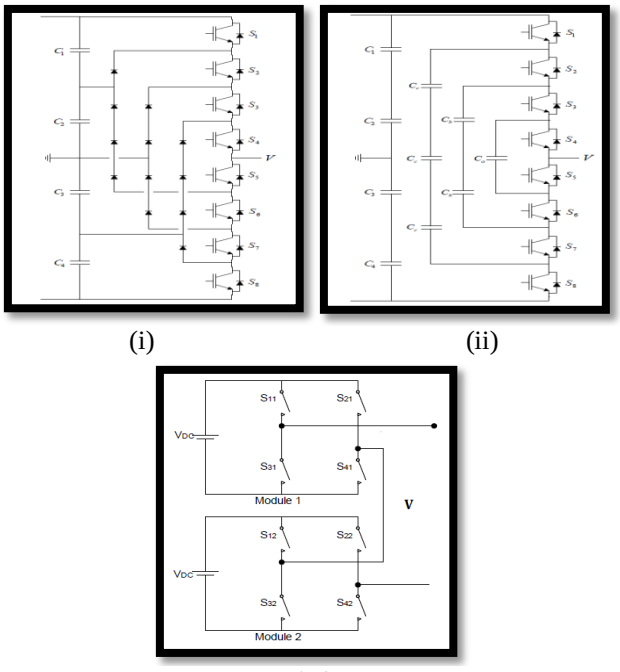
M.Tech Student, Dept. of Electrical Engineering, Tripura University (A Central University), Agartala, India[2,3]

Abstract: For smooth running of the electronic appliances we need high quality AC power. The quality of the AC output power increases as the level of the inverter increases. But with the increase of the level, the number of switches and other associated components also increases in a huge amount. Thus the losses associated with the inverter are also increases. Due to different kind of losses associated with inverters, the efficiency is affected tremendously. Therefore, for improved and efficient multilevel inverter design, the number of switches has to be reduced as much as possible. In this paper, an innovative approach of designing multilevel inverter is proposed, which can increase the generation of two-levels of output voltage by increasing only one switch. This paper explains nine-level single-phase multilevel inverter with this innovative approach, using only eight switches.

Keywords: Multilevel Inverter, Level generator section, Polarity changer section, H-Bridge, IGBTs with anti-parallel diode, IGBTs without anti-parallel diode, MATLAB SIMULINK software.

I. INTRODUCTION

Now-a-days multilevel inverters are become the mother tree for fruit full output of all electronics appliances. But in conventional multilevel inverter topologies (i) Diode Clamped (DC) (ii) Flying Capacitor (FC) and (iii) Cascaded H-Bridge (CHB) [1],[2],[3], as the number of level increases it requires more number of power switches, clamping diode, flying capacitor and associated components respectively. These three conventional multilevel inverter topologies are shown in figure 1.



(i) (ii)

(iii)

Fig. 1. 5 Level (i) Diode Clamped (DC) Inverter
(ii) Flying Capacitor (FC) Inverter and
(iii) Cascaded H-Bridge (CHB) Inverter

Furthermore, this may increase the installation area, cost of the inverter and complex control circuits. Therefore, to overcome the problem of using large number of switches in conventional multilevel inverters, this paper takes a step forward to the development of multilevel inverters family by reducing the number of switches to a large extent without hampering the output voltage quality. For the last few years many researchers take initiative in the field of reduced switch multilevel inverter [4],[5] but this paper demonstrate the best possible design of the higher level multilevel inverter topology with less number of switches, up to the date.

II. PROPOSED TOPOLOGY

In this proposed topology, there are basically two portions in the circuit; one portion called level generator and another one is called polarity changer. In the level generator portion, switches are connected in parallel with each switch is in series connected to separate DC voltage sources in such a manner, where all the DC voltage sources are in series connection. And in the polarity changer portion the circuit is composed of four power switches with H-bridge circuit connection. The only condition is that, the same switches in same leg of H-bridge should not be turned on simultaneous in order to avoid the short circuit with DC source.

A. Proposed Circuit Analysis

In level generator section when switch S1 is only on and switch S2, S3, S4 are off then V_{dc1} voltage is appeared across the load of the polarity changer portion of the inverter circuit.

Similarly when switch S2 is only on and switch S1, S3, S4 are off then (V_{dc1}+V_{dc2}) voltage; when switch S3 is only on and switch S1, S2, S4 are off then (V_{dc1}+V_{dc2}+V_{dc3}) voltage; when switch S4 is only on and switch S1, S2, S3 are off then (V_{dc1}+V_{dc2}+V_{dc3} +V_{dc4}) voltage is appeared across the load of the polarity changer portion of the inverter circuit.

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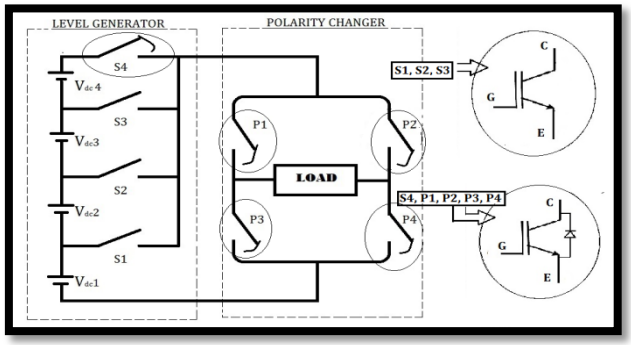

Fig. 2. Proposed 9-Level Inverter with R-L Load Using Only 8-Switches

The operational logic behind the polarity changer portion is that, when (P1, P4) are on and (P2, P3) are off, the load voltage is positive; whereas, in the case of (P1, P4) are off and (P2, P3) are on, the load voltage is negative.

Both the positive and negative levels synthesized by the H-bridge circuit, at resistive load (Vo, Load) synthesized stepped output voltage level will be obtained as

$$Vo = \begin{cases} \sum_{i=1}^{m} Vdci \ , \ P1, P4 = 1 \\ \sum_{i=1}^{m} -Vdci \ , P2, P3 = 1 \end{cases}$$

Practically every electrical load has some inductance. Therefore, when current is flows from dc voltages to load through switches, the inductor in series with the resistor is charged up. After that when switches are off, inductor starts discharging. If this discharging current of inductive load dose not finds any means to flows through and completes its path, output voltage waveform is distorted and the load voltage quality decreases.

Therefore, in proposed inverter topology with R-L load some special kind of IGBT switches which comes along with an anti-parallel diode are used for switch S4, P1, P2, P3 and P4. And for the rest switches of level generator section IGBT switches without anti-parallel diode are used. The anti-parallel diode of the switches S4, P1, P2, P3 and P4 conducts during the time of inductive current discharge.

9-level proposed multilevel inverter

In a 9-level proposed multilevel topology:
n=9
Therefore:
Number of DC voltage sources = (n-1)/2 = 4
Number of switches (IGBT without anti-parallel diode) = [(n-1)/2] -1 = 3
Number of switches (IGBT with anti-parallel diode) = 5

B. Power Stage Operation

In this section, 9-level symmetric multilevel inverter is explained to understand the proposed topology. In order to provide more number of output voltage steps with minimum number of switches by using proposed symmetric topology as shown in figure above, the magnitude of the each steps are calculated for 9-level inverter is explained in two sections below.

• Voltage level calculation for level generator section:

Basically the level generator sections make it possible to increase the voltage level across the load in the polarity changer portion step by step. For every step increments in the load voltage, one switch has to be on in the level generator section. To obtain a nine level output voltage, the mathematical equations are expressed as

$$S1=V_{dc1}$$
$$S2=V_{dc1}+V_{dc2}$$
$$S3=V_{dc1}+V_{dc2}+V_{dc3}$$
$$S4=V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$$

• Voltage level calculation for polarity changer section:

The main section of this proposed inverter, where actually the load voltage inversion take place is the polarity changer section. In this polarity changer section the different voltage levels generated from the level generator section, changes their polarity from positive to negative and negative to positive according to switching timing of the four switches in the polarity changer section.

To obtain positive and negative output voltage, the mathematical equations are expressed as

$$P1+P4 = +\sum_{n=1}^{4} Vdcn$$
$$P1+P4 = -\sum_{n=1}^{4} Vdcn$$

Where n=Sn (i.e., S1, S2, S3, S4) is the switch from the level generator section.

C. Switching States of Proposed Topology

TABLE I: SWITCHING STATES OF 9-LEVEL PROPOSED

Switching States								Voltage Level at $V_{O, Load}$
S1	S2	S3	S4	P1	P2	P3	P4	
1	0	0	0	1	0	0	1	V_{dc1}
0	1	0	0	1	0	0	1	$V_{dc1}+V_{dc2}$
0	0	1	0	1	0	0	1	$V_{dc1}+V_{dc2}+V_{dc3}$
0	0	0	1	1	0	0	1	$V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$
0	0	0	0	1	1	0	0	0
1	0	0	0	0	1	1	0	$-V_{dc1}$
0	1	0	0	0	1	1	0	$-(V_{dc1}+V_{dc2})$
0	0	1	0	0	1	1	0	$(V_{dc1}+V_{dc2}+V_{dc3})$
0	0	0	1	0	1	1	0	$(V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4})$

III.MATLAB SIMULATION

Proposed inverter model for 9-level with only 8 switches is designed here using MATLAB simulation and is shown in the figure 3. An inductive load of L= 10mH with resistive load of R=100 ohms is used here as a load.

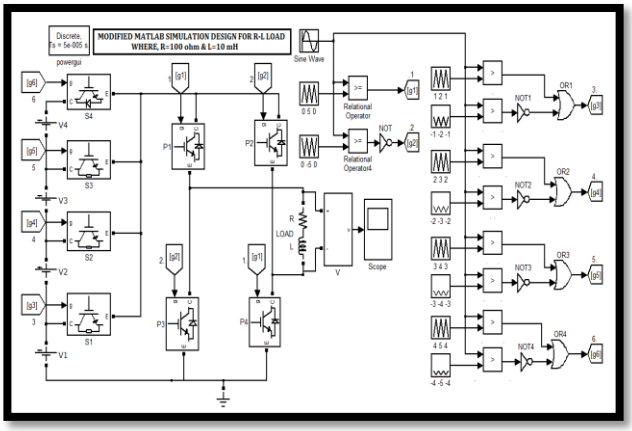

Fig. 3. MATLAB Simulation Design of 1-Phase 9-Level Inverter for R-L Load

For designing this circuit, 5 IGBTs with anti-parallel diode, 3 IGBTs without anti-parallel diode and 4 dc voltage sources each rated with 100 V is used. For turning on IGBT switches it needed pulse signal on IGBT gate terminal. Here for gate pulse of IGBT, Sine Pulse Width Modulation technique is used.

For implementation of this SPWM technique [6],[7] in this proposed circuit, one sine wave of amplitude 5 with 50 Hz frequency and 10 triangle wave-forms with different amplitudes needed. Also 10 rational operator, 5 NOT gate and 4 OR gate needed.

IV. SIMULATION RESULT

After running the MATLAB simulation model shown in figure 3, the visible single-phase 9-level approximately sinusoidal output voltage graph with respect to time is appear in the scope, which is shown in the figure 4.

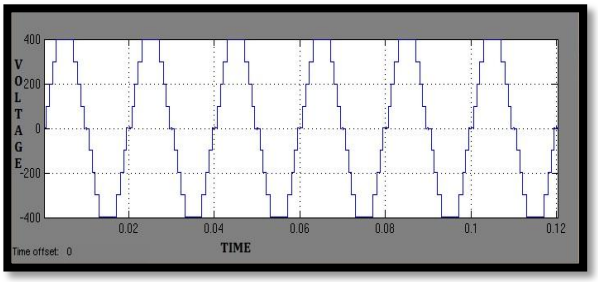

Fig. 4. 1-Phase 9-Level Output Voltage Simulation Result for R-L Load

V. CONCLUSION

In this paper, an innovative approach of designing multilevel inverter is proposed, which uses reduced number of switches. As the number of power switches are reduced here, it is an approach of increasing the efficiency of multilevel inverter by reducing the switching losses. At the same time, this approach gives fruit full results in area of inverter cost minimization and installation area reduction.

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BIOGRAPHIES

Sangita Das Biswas completed M.tech in Electrical Engineering in 2003 from University of Calcutta, Kolkata, West Bengal, India. Now she is serving as Assistant Professor in Tripura University, Suryamaninagar, Agartala, Tripura, India from 2005 onwards. Research interests include Multilevel Inverters, Electrical Power Converters, FACTS devices.

Moumita Saha received B.E degree in Electrical Engineering from Tripura Institute of Technology, Narsingarh, Tripura in the year 2014. She is currently pursuing M.Tech in Tripura University, Suryamaninagar, Agartala, Tripura. Her research interests include Multilevel Inverters, Electrical Power Converters, FACTS devices, Harmonics.

Priyanka Debbarma received B.E degree in Electrical Engineering from Tripura Institute of Technology, Narsingarh, Tripura in the year 2014. She is currently pursuing M.Tech in Tripura University, Suryamaninagar, Agartala, Tripura. Her research interests include Multilevel Inverters, FACTS device.