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FPGA Based Image Enhancement Algorithm for Object Detection and Counting

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Abstract: Countless advantages with respect to performance and functioning for executing applications for image processing are divulged by FPGAs (Abstract-Field programmable gate arrays). Elaborating and developing the particular algorithms in order to find a solution for the problems related to image processing is just a single facet of FPGAs' utilization; these algorithms must then undergo mapping to the FPGA. Image processing is a very important application nowadays it is utilized in many areas such as carbon-dating, army, medical etc. Algorithms present in FPGA's can be utilized to perform many operations on image like contrast stretching, brightness manipulation, operating threshold and real time enhancement of image. When it comes for implementation using Verilog codes is suitable to perform the operations that gives the favourable results and helps in enhancing the image quality and helps in counting the objects through the pixels.

Keywords: FPGA, digitally enhanced image, Verilog, object counting.

I. INTRODUCTION

In recent days the demand for quality image is raised and in order to meet this demand there is necessity for captivating logic, image quality is main criteria in many fields that can be art, medical and DSP's, but meeting this demand is herculean task and must be tackled in cautious way such that it meets the demand of the user at all levels of processing methodology followed in enhancement of image.

Object detection and counting is main part of enhancing the image. Counting the number of images before enhancing is better way of handling the situation and by doing that. The image enhanced will have some compatibility and similarity to the original image. In simple words we can say that has sharpening the edges and boundaries of the image and beautifying the particular area / part of that image by doing that one can enumerate the pixels present in images.

The domains where digital image processing can be implemented and administrated are quite miscellaneous as well as diverse. In order to apprehend the scope and extensiveness of this particular field so that a fundamental understanding can be developed regarding applications of image processing entails a rigorous categorization of images on the basis of what source they were extracted from, for instance electromagnetic energy spectrum (X-ray) or acoustic and ultrasonic, as well as electronic or synthetic images that were separately produced by the utilization of computers [1]. These sorts of applications comprise of various dissimilar processes where augmentation of image quality as well as Object detection are also included.

It is of high significance to take into account that this kind of processing inquires about the resources used, such as memory availability or even specifically connected peripheral devices that are required for the processing power.

Not all of these things can be found on every single common-place Computer that is used for generic purposes and usually the concerned procedures or processes are inefficient because of various other problems. Employing hardware that is specific for particular applications such as ASICs or FPGAs, better results and outcomes can be generated via the use of this software. Today, the technology of VLSI (Very Large Scale Integrated) provides solutions regarding the administration of highly complex alternative hardware [2].

Two highly dissimilar elements are there that are utilized for the betterment or augmentation of images, spatial frequency along with spatial domain approach. One of the approaches is founded on frequency found on image transfiguration or transformation that in turn is on the basis of mathematical transfiguration or transformation as well as the approach or attitude of spatial domain. All of this is dependent on the pixel

The unassuming and straightforward but still useful operations for the augmentation of images in spatial domain include; sieving along with stretching containing contrast and transfiguration or transformation of negative images. It also comprise of calculation of brightness and histogram equalization as well as operations conducted right on threshold and filtering or sieving through

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operations. All of these abovementioned techniques and methods are defined as the image processing point operations. The permeation founded on high pass as well as low pass will be considered a part of the segment of frequency domain. Manoeuvrability is the biggest advantage that is afforded by the betterment or augmentation of an image.

II. LITERATURE SURVEY

The use of MATLAB turns into a challenging task via the fixture of a desired or required computer for all the facilities. A great alternative to this is to frame a separate and independent design that is founded on hardware designed with desirable adaptation and habituation of resource as well as mobility in mind. By the utilization of software facilitates that can be edited, easy and accessible facilitation of computing algorithms of a particular object and hence the performance can be upgraded and advanced so the processing as well as time needed to calculate and compute will be greatly minimized.

To facilitate the proper utilization as well as employment of hardware, countless scientific approaches and attitudes are provided in the literature. They include FPGA (Field programmable gate arrays) along with ASIC (Application specific integrated circuits) and DSP (Digital signal processor) and so on. Via the designs and frameworks founded on ASIC's, the desired performance can be generated. If after it is all assembled and any unlikeness arises it will not be programmable. The DSP microprocessors are not very economical.

A technique of automatic cell counting founded on images that are microscopic was introduced by Xiaomin Guo and Feihong Yu [3]. Information obtained via histogram is employed in order to compute adjustable threshold value of both lower and upper. This value is then utilized for segmentation of background as well as objects. Flood fill method impact stuffs up the regions around objects. It is also utilized to mark as well as segregate an image's segments. A blob is a range of pixels that is in contact with the similar logical region or state. Every pixel that an image contains that is related, in a state that is foreground, to a particular blob. The remaining pixels are found or can be located in the background. Analysis of a blob or examination is employed to expose blobs that a particular image contains so that chosen measurement of a particular blob can then be carried out. Blob examination or analysis comprises of an ongoing series or a pathway of operations that are being processed as well as examination of the functions that provide the information required or needed regarding any 2D figure that an image might contain. If and when the measurement of a blob is found to be the scope of an area's upper threshold that is undergoing this analysis, the blob's segmentation will be done by the algorithm of 'K-means clustering.' Via computing the cells' quantity that are present in each blob, total cells in the entire image is obtained. The outcome of this indicates that maximum relative error is 1.33%, minimum relative error is 0% and the average relative error is 0.46%. Via the utilization of the Hough transform, a technique for automatic counting of the red blood cell was demonstrated by Venkatalakshmi. B et al. [4]. In order to estimate or approximate red blood cells, the algorithm comprises of five steps that are; 1) input image acquisition, 2) pre-processing, 3) segmentation, 4) feature extraction and 5) counting. In the step of pre-processing, an HSV image is obtained from the original blood smear via conversion. As bright components are unambiguously indicated by the Saturation image, it is employed additionally for examination. Segmentation's very first step is to recognize both lower as well as upper threshold via information obtained through the histogram. Two binary images are then obtained by the division of saturation image on the basis of this information. Morphological area closing is used in the image of a pixel value that is lower as well as dilation in the morphological sense as well as area terminating point is utilized for the image of a pixel value that is higher. XOR operation of the morphological type is used to apply to two images that are binary as well as Hough transform (circular) is used in order to obtain RBCs.

The use of FPGA'S is the one alternative that is much better for all these tribulations. On the basis of the user's necessities and requirements, various different methods and techniques are programmable in interconnects as well as inherently built inside FPGA, the logical blocks. The characteristic or the feature regarding reconfiguration is FPGA inherent and it helps pipeline the functionality. It costs less to manufacture FPGA. FPGA's can be programmed when facilitated by VHDL as well as Verilog HDL. Verilog HDL is what every single algorithm is founded on that is discussed or mentioned in this particular paper. Verilog HDL is employed because divergences can effortlessly be recognized while the processes of predecessor error checking are conducted.

III. ALGORITHM STEPS

The most notable point is there should zero attachment to the background by an object. In this, for maintaining an accurate count of objects, some initial calculations are needed. Following four improving techniques are employed:

- Brightness Manipulation
- Contrast stretching
- Real time approach
- Operating threshold

Brightness Manipulation:
Brightness manipulation is useful to enhance the brightness of image when image is captured in low light condition. After brightness manipulation it is easy to interpret the information in image easily.

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Brightness manipulation operations are commonly used for increasing and decreasing Brightness. After brightness manipulation, dark image may become brighter or bright image may become dark .If we add the constant value in pixel value of image, then brightness manipulation operation increase brightness and similarly subtraction operator reduces the brightness as explained by following equation.

$$F(x,y) = \begin{cases} G(x,y) + t \text{ if } G(x,y) + t \leq 255 \\ 255 \quad \text{if } G(x,y) + t > 255 \end{cases}$$

Where $t \geq 0$

$G(x,y)$ – Gray Level for Input Pixel

$F(x,y)$ –Gray Level for Output Pixel [5]

Operating threshold:

Thresholding of image means converting gray level information of image to two-level information. If the object presented in the foreground has dissimilar gray levels than the background it is surrounded by, 'image thresholding' is a viable tool for this segmentation or segregation. Threshold operation is defined employing following equation where a_{th} is the threshold value which is important for the separation of the pixel values in two classes.

$$F(x,y) = \begin{cases} G_0(x,y) \text{ for } G(x,y) < a_{th} \\ G_1(x,y) \text{ for } G(x,y) \geq a_{th} \end{cases}$$

Where $G(x,y)$ – Gray Level for Input Pixel

$F(x,y)$ –Gray Level for Output Pixel

a_{th} - Threshold Value

By using equation above equation, from the input image, values of each pixel are replaced by the successive pixel in the destination image using $G_0(x,y)=0$ & $G_1(x,y)=1$.

Contrast stretching:

Contrast stretching is a technique in which some or all of the intensity value in the original image are stretched out to occupy a larger range of values to easily interpret the information in image. It can be explain by following equation.

$$F(x,y) = \begin{cases} t_0 \text{ if } G(x,y) < g_0 \\ G(x,y) \text{ if } g_0 < G(x,y) < g_1 \\ t_1 \text{ if } G(x,y) > g_1 \end{cases}$$

Where $G(x,y)$ – Gray Level for Input Pixel

$F(x,y)$ –Gray Level for Output Pixel

t_0, t_1 - Constant values

Contrast stretching used to increase the brightness of object compare to background so that it can be easily interpreted. Contrast stretching is commonly used in application such as CT scans for enhancing the quality and contrast of medical images.

Real time approach:

In the real time approach the image obtained is restructured and enhanced with view of the initial image, the quality of the image obtained after performing above said algorithm will give the exact details of the image and will be helpful in analyzing it in detail.

Counting algorithm:

After the thresholding objects and background are separated or segmented. Hence it becomes simpler to locate group of pixels contained in an image that somehow belong together for finding out number of objects in image. By counting number of white pixels, numbers of objects are counted. Number of objects in image is shown by using LED's. Up to 256 objects can be shown by using LED's.

IV. IMPLEMENTATION

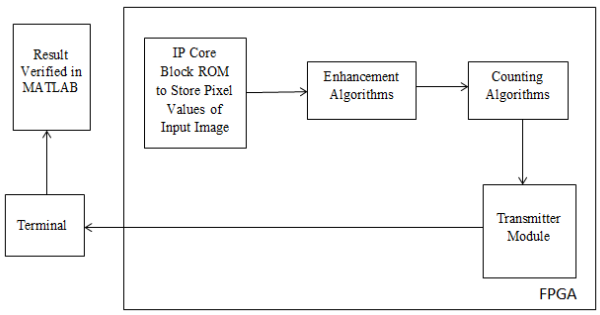

Fig.1. Generalized block diagram of the system

A system's generalized block diagram to administrate the computing of objects algorithm is as shown in Fig.1. It consists of IP core ROM to store the input images, in this proposed work the size of input image is 128*128 so to store these many pixels the ROM size is also kept same as input image size. Enhancement algorithm block consist of algorithm of three enhancement techniques. Firstly, the input image gets enhanced by using brightness manipulation to increase the brightness of image as image is taken in low light then contrast stretching was done so that objects can be interpreted clearly and finally by using thresholding operation, separation the objects from background was carried out. By counting number of white pixels, numbers of objects are counted. Output of algorithm block is sent through hyper terminal which necessitates the use of transmitter block prior to hyper terminal. Finally output image is verified in MATLAB. The numbers of objects in image are indicated by using led on the FPGA.

A. Core IP (Generator Memory Block)

The Core IP block ascribes to the initial logic functions pre-processed and can be made part of an overall framework or design. A generator core system forms built

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cores which provide competent area optimization as well as higher levels of performance. A lone Core IP is mentioned here and Core IP ROM is utilized in order to store the image that was used as the input.

B. UART Transmitter

Through a serial line's aid, the receiver that is universal as well as asynchronous along with transmitter (UART) is utilized data parallel form transmission. Modules, that were inbuilt and three in number, were comprised in UART; 1) the module of receiver, 2) transmitter and 3) a generator for computing the baud rate. Start bit '0' and then data bits followed optional parity bit at end stop bit.

Fig 2 Frame format

Xilinx FPGA Board utilized is showcased in figure 3. It is administrated in Xilinx Board with Led having parallel port connections. LED is utilized for showcasing the FPGA generated output to processing element in order to verify the result shown in the image.

Fig 3 FPGA image showing coin detection by LED's

V. RESULTS

A FPGA family will be familiarized for the functioning of quantifying object algorithms along with algorithms that are hardware dependent. The tool required for relocating as well as producing will be ISE 14.7 version of Xilinx. In order to verify, image's measurements will be of 128*128 Gray-level based pixel resolution. In order to relocate signal, serially, the following path will be followed; a start bit then a data bit size of eight and then finally a stop bit. After the relocation of all the bits is done, the statement for end signal will be released. This is how data is transferred via terminal, from the pc to FPGA Board. This then undergoes processing and then the image processed is usually transferred via the same terminal used before, back in the PC.

Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	26	126,800	1%
Number used as Flip Flops	26		
Number used as Latches	0		
Number used as Latch-thrus	0		
Number used as AND/OR logics	0		
Number of Slice LUTs	14	63,400	1%
Number used as logic	14	63,400	1%
Number using O6 output only	8		
Number using O5 output only	0		
Number using O5 and O6	6		
Number used as ROM	0		
Number used as Memory	0	19,000	0%
Number used exclusively as route-thrus	0		
Number of occupied Slices	4	15,850	1%
Number of LUT Flip Flop pairs used	16		

Fig 4 Device utilization summary

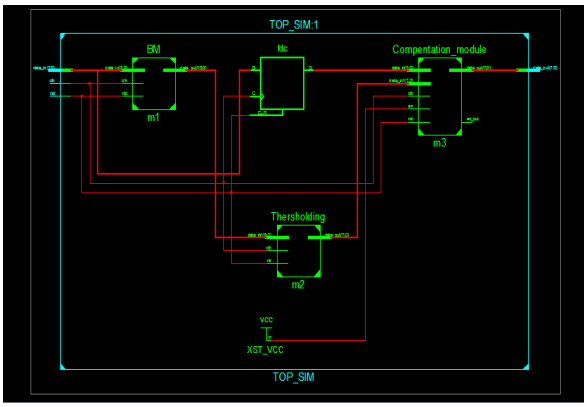

Fig.5. RTL schematic

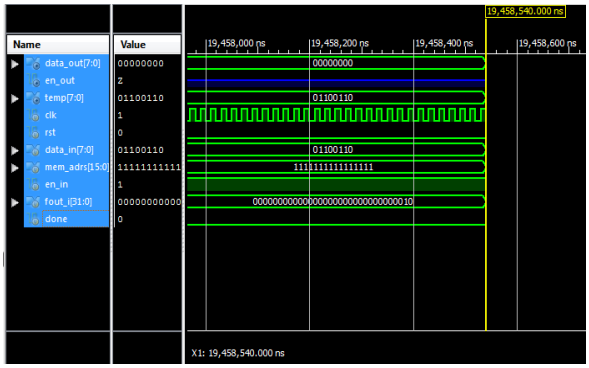

Fig 6 Simulation result of enhanced image

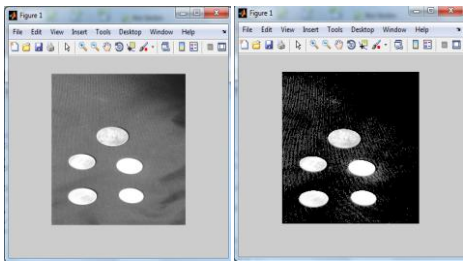

Fig .7. (a) original image (b) Image obtained after enhancement algorithm

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VI. CONCLUSION

The image processing is straightforward in FPGA board when comparisons are drawn with the processors of other types. When the hexadecimal code is employed to encode an image by utilizing MATLAB and from the PC, it is put back into the FPGA Board then later Image brightness along with contrast stretching as well as operating threshold can be effectively altered by employing FPGA dumped Verilog code. The process of reconversion is also smoothly running when this MATLAB milieu is employed. Complications regarding hardware here is primarily interface related (Bluetooth module or serial port) among laptop or personal computer as well as FPGA kit. The code's complex design gets reduced or minimized too via the utilization of algorithm comprising of three steps than any normal edge, detection algorithm employed for the computation of objects.

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