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Low Transition Test Pattern Generation for Minimizing Test Power in VLSI Circuits Using BIST Techniques

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Abstract: In the semiconductor manufacturing industry recently remarkable technological developments like, feasibility of millions of transistors and various other components to be integrated on a Chip with enormous packaging options than it is tested by BIST. The role of the BIST circuit is to reduce the cost by reducing the testing interval and the complexity of testing. The power dissipated in a circuit during testing mode is considerably larger than that dissipated in the operational mode. This increase in power dissipated can be recognized to the decreased correlation between the random patterns generated in the test mode. Hence, the idea behind this paper is to design a DFT circuit that will help in decreasing the switching activities in the test mode in order to limit the power dissipation.

Keywords: Built-In Self-Test, VLSI Testing, LFSR technique, low-power test vector pattern generation.

I. INTRODUCTION

Today's System-On-Chip (SOC) devices contain integration of a large number of processors, different types of memories like SRAM, user defined logic and Digital signal processors, with an increasing count in transistors on a single chip thereby, challenging the design and testing methodologies in vogue [1]. The testing of ICs, today, mandates a new and high-level of competence and accuracy, expecting complete verification through all of the stages of the design process.

It is a known fact that power dissipation in the circuit during the test mode is considerable compared to that in the normal mode. This can be attributed to the correlation existing between consecutive test vectors applied during the normal mode of operation of the circuit. But this is not the case in the test mode. There is no significant correlation between consecutive vectors in the test mode. This automatically means that the primary switching activities will be more in the test mode compared to that in the normal mode and that the power dissipation will be higher in the test mode. Thus, more the transitions between the test vectors more will be the power dissipated. Hence, low power testing is the need of the hour.

One way of circumventing this issue is by the use of Built-In-Self-Test (BIST) architecture. A BIST circuitry is contained as a part of the target system that aids in the verification of the internal functionalities of the particular circuit it is assigned. BIST is a methodology of allowing test logic to be incorporated as a part of the chip itself. The BIST architecture is widely accepted because of its very many advantages like the reduction in test application time, reduction in the cost of generation of test vectors, to allow at-speed testing, to provide an alternative to the expensive Automatic Testing Equipment (ATE) and the reduction in the volume of test data. Also, the overhead area occupied by the BIST in the circuit can be considered negligible in comparison to the size of the target system [2]. The BIST makes the target system independent of any external automatic equipment for testing.

Hence, this proposed method aims to analyse and discuss a circuit that generates test patterns that help reduce the average and peak power dissipation in BIST architecture during testing mode. Also, efforts are made about to bring appropriate modifications to the logical and structural implementation, of the circuit under consideration, in order to reduce the power dissipation even further [3].

II. TEST PATTERN GENERATION

Test patterns are basically a set of inputs (1's and 0's) which, when applied in a circuit, will determine if the circuit is working as per the requirement or if it is faulty

2.1 Need for low power testing

The System-On-Chips platform imposes a challenge in the design and testing methodology. Testing gains the primary significance in terms of issues and expenditure, thereby, demanding a wide range of possible novelties. The area of concentration, here, is power dissipation [4]. In general, the power consumed during the test mode is more than that in the normal mode of operation. This additional power dissipated may pose a threat to the circuitry and can also lead to a breakdown of the chip. This in turns will

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raise the costs, increase the difficulty in verifying the performance of the circuit and thereby reduce the final code. Having leant the above, the necessity of decreasing the power dissipated in a circuit during the test mode is a major milestone for further advancements in VLSI design [5].

A number of reasons can be quoted for the increased power consumption in the circuit during the test mode. Decreased correlation between the test vectors can be sited as the first reason. Normally, a considerable correlation exists between the inputs during the operational mode but may not be the same in the test mode. This decreased correlation in the input during the test mode increases the switching activities, thereby increasing the power dissipation [6]. Secondly, the use of parallel testing process by test engineers in order to reduce the test application time can result in increased power dissipation. The third reason can be attributed to the DFT circuit that is inbuilt in the design for the test mode, which is normally idled during the operational mode, however, is extensively active in the test mode [7].

III. LOW POWER MODELS UNDER CONSIDERATION

3.1 The modelled low power test pattern generator

The primary task in the designing of a BIST circuit is in ensuring low power dissipation during the test mode by reducing the primary switching activities. Here, the low power test pattern generator named LP-TPG adopted in is discussed as an example. Two consecutive random test vectors generated from an LFSR is taken as the base. Considering the base patterns, the circuit is accordingly modeled so as to generate three intermediate test vectors in between the two consecutive random test vectors generated from the LFSR [8]. This introduction of the intermediary vectors helps in reduction of the average power and the peak power since the number of transitions between the two base patterns from the LFSR and number of transitions between the two base patterns including the three patterns inserted from the new model is the same. This directly relates to the minimized power consumption in the new model than that in the conventional LFSR and implies that the correlation between the test vectors generated by LP-TPG is more than the correlation between the conventional LFSR vectors. This technique also takes into deliberation that the randomness of the generated patterns is not reduced [9].

The two consecutive random test vectors generated by the conventional LFSR are named P i^i and P i+1, were in P i = {P i1, P i2, …, P in) and P i+1 = {P i+11, P i+12, …,P i+1n}. Here, n represents the number of transistors that are switched for every clock pulse and are generated as bits at the output. This determines the switching activity of the circuit under test. The three intermediary patterns generated by the introduction of the new Low Power model are named Pk1, Pk2 and Pk3.

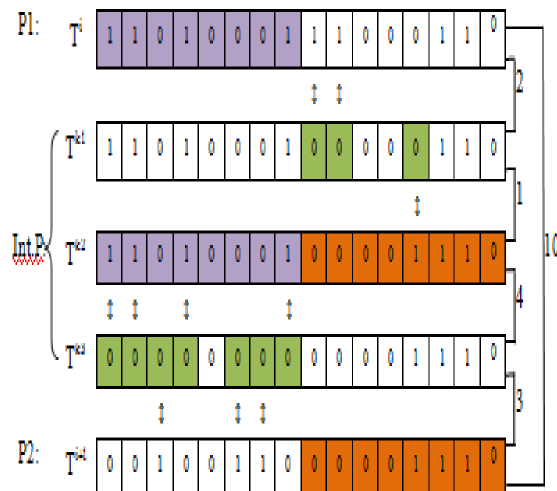

Figure1. An example of intermediate pattern generation

Referring to Figure 1, we observe that Pk2 is generated as the intermediary of Pi and Pi+1, i.e. The first half of Pi and the second half of Pi+1 is combined to form Pk2.

$$PK2=\{t_1^i,......,t_{\frac{n}{2}}^i,t_{\frac{n}{2}+1}^{i+1},......,t_n^{i+1}\}$$

Here, Pk2 is again a random vector because it is obtained from two random vectors only. Once Pk2 is obtained, the bits of Pi and Pk2 are compared to generate Pk1. If a particular bit of Pi is equal to the corresponding bit of Pk2, then the corresponding bit of Pk1 is represented by that particular bit.

For Example, in the 1st bit position, both Pi and Pk2 have bit '1', hence, bit '1' is represented as the 1st bit position for vector Pk1. However, if they are not equal, then the corresponding bit of Pk1 is substituted by R (which is '0') as shown below in this case.

$$t_j^{k1} = \begin{cases} t_j^i & \textbf{if} \quad t_j^i = t^{k2} \\ R & \textbf{if} \quad t_j^i \neq t_j^{k2} \end{cases}$$

Where j ε {1, 2,…, n}, Similarly, Pk3 is generated by the comparison of Pk2 and Pi+1. This method of generating the vectors Pk1 and tk3 is called R-Injection. Here, we observe that the number of switching activities between the vectors Ti and Ti+1 is equal to the sum of switching activities between the & Pk1, Pk1 & Pk2, Pk2 & Pk3 and Pk3 & Pi+1. This is represented as below

$$N_{trans}^{i,k1}+N_{trans}^{k1,k2}+N_{trans}^{k2,k3}+N_{trans}^{k3,(i+1)}=N_{trans}^{i,(i+1)}$$

$$\sum_{j=1}^{n}|t_j^i-t_j^{k1}|+\sum_{j=1}^{n}|t_j^{k1}-t_j^{k2}|+\sum_{j=1}^{n}|t_j^{k2}-t_j^{k3}|+\sum_{j=1}^{n}|t_j^{k3}-t_j^{i+1}|=\sum_{j=1}^{n}|t_j^i-t_j^{i+1}|$$

However, the point to be considered in this place is that the test time, on the whole, and the fault coverage remains the same with the introduction of the intermediary test vectors.

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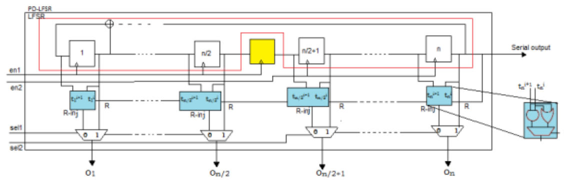

Figure2. Proposed Low Power LFSR (PD-TPG)

Figure 2 shows PD-TPG designed, by integrating the proposed logic with the conventional LFSR, to generate the three intermediary patterns. The circuit consists of an 8-bit external-XOR LFSR with polynomial x^8 + x + 1 and seed = 01001011. Each time the values of first four flip flops are shifted to the right according to the signals the shaded flip holds the value of the 4th flip-flop.

R-Injection circuit - The R-Injection circuit consists of an AND gate, an OR gate and a 2*1 multiplexer. The R-Injection circuit holds the current state and the next state of the corresponding bits of each vector. When both the corresponding bits are equal, the AND and the OR gate generates the same value of the bit. However, when the corresponding bits are not equal, the random bit R is given to the output

Multiplexer – As is known, it consists of two AND gates and an OR gate. The inputs to one of the AND gates are sel signal and the output of the corresponding R-Injection circuit. The other AND gate gets its inputs as sel BAR and the output of the corresponding flip-flop. The output of the AND gate is then ORed to give the final output.

The random vectors are generated with the help of two enable signals (en1 & en2) and to select signals (sel1 & sel2) and is not dependent on the size or the polynomial of the LFSR. Signal Sel1 is connected to the first four multiplexers, and signal Sel2 is connected to the last four multiplexers. The Sel signal selects either the output of the LFSR or the output of the R-Injection circuit accordingly. If Sel = '1', then the LFSR outputs are provided to theOutput and if Sel = '0', then the R-Injection circuit's outputs are available at the final output. Similarly, signal en1 is connected to the first four flip-flops, and en2 is connected to the last four flip-flops. If en = '1', then the respective half of the flip flops to which the en signal is connected are active and the values pertaining to those flip flops are shifted to the right. However, if en = '0', the half of the flip flops to which the signal is connected is in the idle mode and do not shift their values to the right. The circuit also consists of the clock and the Test_en signal that uses the select the Test mode. This circuit generates vectors as are shown and described next.

Step 1: sel1 sel2 = 11, en1 en2 = 10.
When sel1 sel2 = 11, it means that the multiplexer is designed to select the outputs of the LFSR for both halves of the LFSR circuitry. Similarly, When en1 en2 = 10, it means that the first half of the LFSR is active, but the second half is in the idle mode. On this command, the vector Pi is generated.

Step 2: sel1 sel2 = 10, en1 en2 = 00.
When sel1 sel2 = 10, the first half of the LFSR output and the second half of the R-Injection circuit are given to the final outputs. Similarly when en1 en2 = 00, both halves of the LFSR are idle and do not shift values for that clock pulse. These signals are generated vector Pk1.

Step 3: sel1 sel2 = 11, en1 en2 = 10.
In this case when sel1 sel2 = 11, both halves of the LFSR are obtained at the final output and the second half of the LFSR is in the idle mode, whereas the first half of the LFSR is active for en1 en2 = 10 and the bits are shifted to the right. In this case, the values of the four flip flops are shifted to the shaded flip flop. Once this process if completed, the vector Pk2 is generated.

Step 4: sel1 sel2 = 01, en1 en2 = 00.
When sel1 sel2 = 01, then second half of the LFSR outputs and the first half of the R-Injection circuit's outputs are available on the main output, and When the signal en1 en1 = 00 are enabled, both halves of the flip flops are in the idle mode. Vector Pk3 is generated for this procedure.

Step 5: The procedure as in step 1 is repeated here and vector Ti+1 is generated. The above method continues from step 1 through step 5 for as many clock cycles as is required. The complete circuit is controlled by a finite state machine (FSM), as is shown in the below circuit that acts as the gear stick in the generation of the test patterns. The FSM serves as the control unit for the generation of the test patterns by continuing through steps 1 to 4. The inputs to the FSM are test_en and clk. When test_en = 1, the FSM is initiated with step 1 wherein en1 en2 = 10 and sel1 sel2 = 11 and continues till step 4 with the generation of a vector for every clock pulse. As can be observed, the intermediary vectors Pk1, Pk2 and Pk3 are generated between two consecutive random vectors P1 and P2. It is seen that the number of transitions between P1 and P2 are 7. However, the transitions between P1 & Pk1 = 1, Pk1 & Pk2 = 2, Pk2 and Pk3 = 2 and that between Pk3 and P2 = 2. This shows that the switching activities between the test vectors, after the introduction of the three intermediary vectors, has significantly reduced, between the patterns, thereby reducing the average and peak power dissipation.

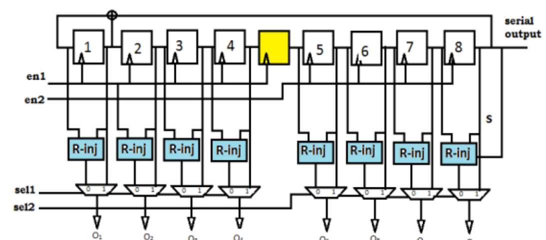

Figure 3. An example of PD-LFSR using a 8-bit LFSR

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TABLE 1

#clk	Pattern	En1 en2 sel1 sel2	LP-LFSR
1	T^1	1 0 1 1	1010 1011
2	T^k_1	0 0 1 0	10101111
3	T^k_2	0 1 1 1	10100101
4	T^k_3	0 0 0 1	11110101
5	T^2	1 0 1 1	01010101

Figure 3(a) shows an example of the PD-TPG using an 8-bit LFSR with polynomial X^8+X+1 and seed=01001011. Table 1 shows the output of the PD-TPG for R=1.

IV. MODIFIED LOW POWER TEST PATTERN GENERATOR

Three approaches aimed at reducing power consumption have been analyzed and discussed in this section. All of these approaches are concentrated on modifying the behavioral model of the LP-TPG under consideration.

In the original circuit, the R-Injection circuit is responsible for introducing a random bit if the corresponding bit position has different values. In order to achieve this, the R-Injection circuit consists of an AND gate, and OR gate and a 2*1 multiplexer as mentioned in figure 5.

The R-Injection circuit takes the current input and output values of D-ff of the LFSR circuit as input. These bits are ANDed and ORed inside the R-inject circuit. Hence the output of AND gate holds high value when both current input and output value of D-ff are high.

While OR gate holds high value when either current input or output of D-ff is high. Then the outputs of the AND and OR gates are inputted to a 2:1 MUX, whose select pin (R) is inputted by the serial output [SO] of the main circuit.

Hence, in the circuit, the select input randomly assigns either first or second input of the MUX to it's output pin. The status of the select pin of the MUX is entirely depended on the status of output of D-ff which holds the MSB of the generated pattern.

V. RESULTS

In Table 2 result shows that initially by adding an R-injector circuit for full Subtractor benchmark circuit, we can see that Total power reduced by 3.91 % compared to conventional LFSR, then by adding Bit Interchange circuit it reduced to 22.26 % compared to conventional LFSR. Similarly, for Full adder 3.14 % reduction by adding an R-injector circuit and 6.61 % reduction by adding Bit Interchange circuit.

Cadence tool simulated output shown in figure 4

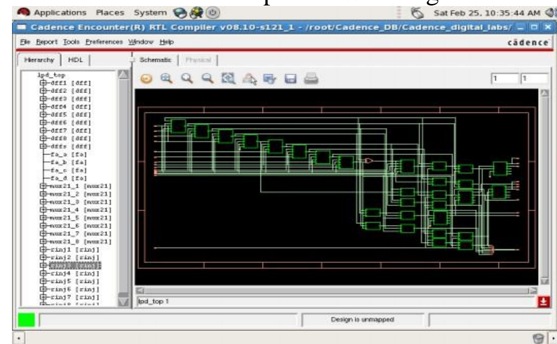

Figure 4. Simulation Output

The pie chart in figure 5 shows the total power obtained during the simulation:

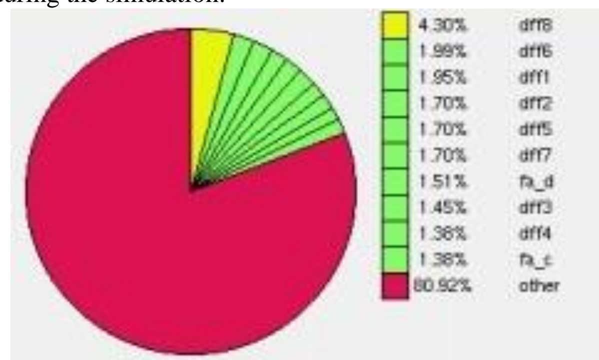

Figure 5 Pie Chart

TABLE 2 .EXPERIMENTAL RESULTS OF NEW PD-TPG COMPARE TO CONVENTIONAL LFSR

Circuits	Conventional LFSR			LFSR+RI (Method-1)			PD-TPG (Method-2)		
	LP(nw)	DP(nw)	TP(nw)	LP(nw)	DP(nw)	TP(nw)	LP(nw)	DP(nw)	TP(nw)
Full sub	22.204	9970.13	9992.334	22.204	9578.883	9601.087	22.204	7745.385	7767.589
Full adder	22.140	11922.20	11944.343	22.140	11657.899	11680.039	22.140	11 311.123	11333.263
Binary to Gray	18.588	1549.09	1568.09	18.588	1390.654	1409.242	18.588	1875.990	1894.578
Gray to binary	18.588	4640.580	4659.169	18.588	3207.115	3225.703	18.588	3352.715	3371.304

VI. CONCLUSION

This paper presents a new PD-LFSR to reduce the average and peak power of a circuit during the test mode. By increasing the correlation between the test pattern, the switching activity in the circuit under test and eventually the power consumption is reduced. Additional intermediate test patterns inserted between the original random patterns reduces the PIs activity, average and peak power. The experimental results of Full Subtractor indicate up to 22.25 % reduction in total power compare to conventional LFSR It is concluded that low power LFSR is very much useful for power optimization of BIST.

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