



Implementation of Digital Circuits Using Reversible Logic

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Abstract: Reversible logic has presented itself as a prominent technology which plays an imperative role in Quantum Computing. Quantum computing devices theoretically operate at ultra high speed and consume infinitesimally less power. Research done in this paper aims to utilize the idea of reversible logic to break the conventional speed-power trade-off, thereby getting a step closer to realise Quantum computing devices. To authenticate this research, various combinational and sequential circuits are implemented such as a 4-bit Ripple-carry Adder, (8-bit X 8-bit) Wallace Tree Multiplier, and the Control Unit of an 8-bit GCD processor using Reversible gates. The power and speed parameters for the circuits have been indicated, and compared with their conventional non-reversible counterparts. The comparative statistical study proves that circuits employing Reversible logic thus are faster and power efficient. The designs presented in this paper were simulated using Xilinx 9.2 software.

Keywords: Reversible logic, Quantum Computing, highspeed, less power, speed-power trade-off, Ripple carry adder, Wallace tree multiplier, GCD processor, non-reversible counterparts.

I. INTRODUCTION

Reversible logic is widely used in low power VLSI. Reversible circuits are capable of back-computation and reduction in dissipated power, as there is no loss of information [1]. Basic reversible gates are employed to achieve the required functionality of a reversible circuit. The uniqueness of reversible logic is that, there is no loss of information since there is one-to-one correspondence between inputs and outputs. This enables the system to run backwards and while doing so, any intermediate design stage can be thoroughly examined. The fan-out of each block in the circuit has to be one. This research paper focuses on implementation of reversible logic circuits in which main aim is to optimize speed of the design. A Reversible adder is designed using basic reversible gates. Using this adder, an 8-bit reversible ripple-carry adder is devised and then compared with the conventional 8-bit adder in terms of speed, critical paths, hardware used. Then using the same reversible adder, a Wallace tree multiplier has been implemented, and compared with the conventional Wallace tree multiplier. With the known fact that sequential circuits are the heart of digital designing, the design for the control unit of a reversible GCD Processor has been proposed using Reversible logic gates.

II. REVERSIBLE LOGIC

Boolean logic is said to be reversible if the set of inputs mapped have an equal number of outputs mapped i.e. they have one-to-one correspondence. This is realized employing reversible gates in the designs. Any circuit having only reversible gates is capable of dissipating no power [2].

Goals of Reversible Logic:

- A. Quantum Cost: Quantum cost of a circuit is the measure of implementation cost of quantum circuits. More precisely, quantum cost is defined as the number of elementary quantum operations needed to realize a gate.
- B. Speed of Computation: The time delay of the circuits should be as low as possible as there are numerous computations that have to be done in a system involving a quantum processor; hence speed of computation is a very important parameter while examining such systems.
- C. Garbage Outputs: Garbage outputs are those output signals which do not contribute in driving further blocks in the design. These outputs become redundant as they are not required for computation at a later stage. The garbage outputs make the system slower; hence for better Efficiency it is necessary to minimize the number of garbage outputs.
- D. Feedback: Looping is strictly prohibited when designing reversible circuits.
- E. Fan-out: The output of a certain block in the design can only drive at most one block in the design. Hence it can be said that the Fan-out is restricted to 1.

III. REVERSIBLE GATES

There are many reversible gates such as Feynman, Toffoli, TSG, Fredkin, Peres, etc [3]. As the universal gates in boolean logic are Nand and Nor, for reversible logic, the universal gates are Feynman and Toffoli gates.



1. Feynman Gate: Feynman gate is a universal gate which is used for signal copying purposes or to obtain the complement of the input signal. The block diagram of Feynman gate is shown in fig.1:

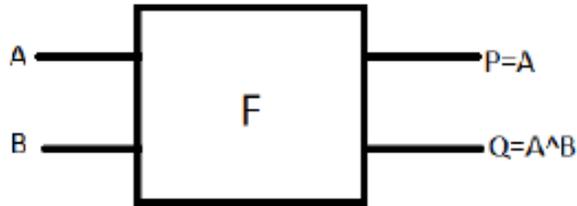


Fig. 1: Feynman Gate

2. Fredkin Gate: It is a basic reversible 3- bit gate used for swapping last two bits depending on the control bit. The control bit here is A, depending on the value of A, bits B and C are selected at outputs Q and R. When A=0, (Q=B, R=C) whereas when A=1, (Q=C, R=B). Its block diagram is as shown in fig. 2:

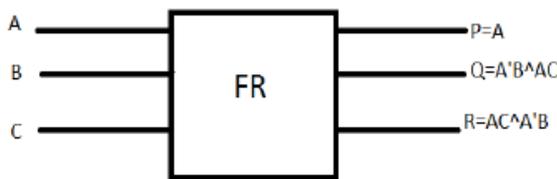


Fig. 2: Fredkin Gate

3. Peres Gate: It is a basic reversible gate which has 3- inputs and 3-outputs having inputs (A, B, C) and the mapped outputs (P=A, Q=A^B, R=(A.B)^C). The block diagram is as shown in fig. 3:

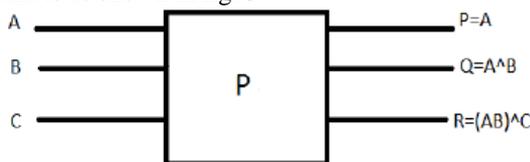


Fig. 3: Peres Gate

4. Toffoli Gate: Toffoli gate is a universal reversible gate which has three inputs (A, B, C) mapped to three outputs (P=A, Q=B, R= (A.B)^C). The block diagram of Toffoli gate is shown in fig. 4:

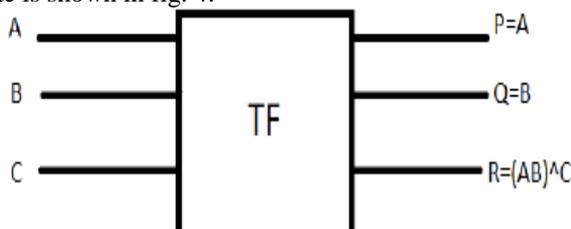


Fig. 4: Toffoli Gate

5. TSG Gate: TSG gate is a reversible gate which has four inputs (A, B, C, D) mapped to four outputs (P=A, Q=A^B, R=A^B^D, S=(A^B)^D^AB^C). The block diagram of TSG Gate is shown in fig. 5:

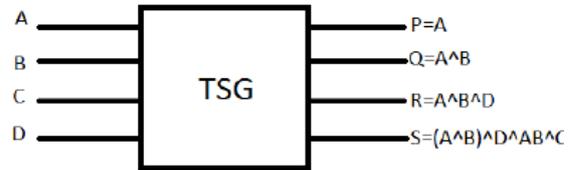


Fig. 5: TSG Gate

IV. REVERSIBLE 4- BIT FULL ADDER

The gate used in implementing a reversible ripple-carry full adder is the TSG gate [4]. The TSG gate functions like a full adder. A reversible ripple-carry adder is faster than the non-reversible adder, since the computation of carry in a reversible adder does not require the computation of previous stage carry (as indicated in the critical paths).

When previous stage carry is being forwarded in the reversible adder, the computation of previous stage carry and computation regarding sum is done simultaneously whereas in an irreversible adder the next stage carry cannot start any computation till previous stage carry is fully generated. The critical paths of 4bit reversible and irreversible ripple-carry adders are as shown in fig.6 and fig.7.

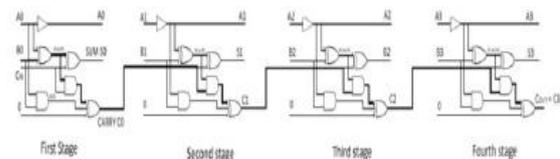


Fig. 6: Critical Path of 4-bit reversible adder

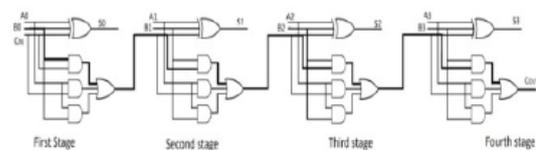


Fig. 7: Critical Path of 4 bit irreversible adder

Furthermore, various parameters of reversible and non reversible adders were observed and compared and are tabulated in Table 1.

Table 1: Comparison of Reversible and Irreversible RCA

Parameter (Virtex5 XC5VLX30 family)	8bit Reversible RippleCarry Adder	8bit Irreversible RippleCarry Adder	Improvement For Reversible Circuit (%)
Time delay	5.062ns	5.547ns	8.74%
Power	267.18mW	290mW	7.87%
Area (No. of LUTs)	11	13	15.38%

V. WALLACE TREE MULTIPLIER

A **Wallace tree** is an efficient hardwired implementation of a digital circuit that multiplies two integers [5]. The Wallace tree has three steps:

1. Every bit of the multiplicand is multiplied (i.e. AND) by every bit of multiplier, thus yielding n^2 results (for



n X n multiplication). Depending on position of the multiplied bits, the wires carry different weights, i.e. weight of bit carrying result of a5b6 is 65.

2. The number of partial products is reduced to 2 by layers of full and half adders.
3. The wires are grouped in two numbers, and added using a conventional adder.

The circuit diagram of Wallace tree multiplier using reversible gates is shown in fig. 8.

Implementation of reversible and irreversible 8bit X 8bit Wallace tree multipliers were done and the comparison is as shown in table 2

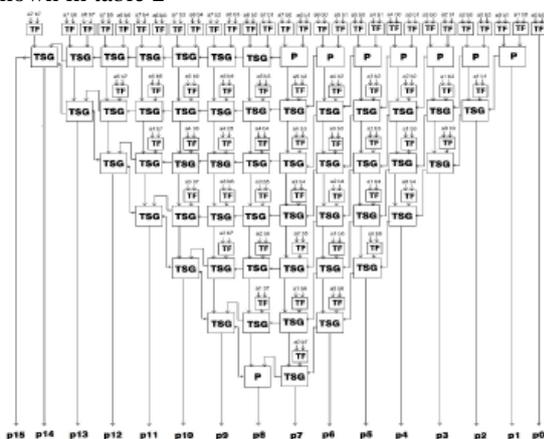


Fig. 8: 8X8 reversible Wallace tree Multiplier

Table 2: Comparison of Reversible and Irreversible Wallace Tree Multiplier

Parameter (Virtex5 XC5VLX30 family)	8-bit Reversible Wallace tree multiplier	8-bit Irreversible Wallace tree multiplier	Percentage Improvement For Reversible multiplier
Time delay	9.548ns	11.162ns	14.46%
Power	266.84mW	380.86mW	29.94%
Area (No. of LUTs)	103	117	11.97%

VI. DESIGN OF CONTROL UNIT FOR GCD PROCESSOR

To illustrate the classical and reversible approaches to the Sequential Control Unit Design, reversible logic is employed for a special purpose processor that computes the GCD of two numbers. This GCD processor incorporates standard Euclid's Algorithm involving Subtract-Compare-Swap operation of two numbers. The basic principle is to subtract smaller of the two numbers repeatedly from the other number until we get the number that divides another [6].

A. Control Unit

Control unit of GCD processor generates the control signals to manipulate the operations in Data-path.

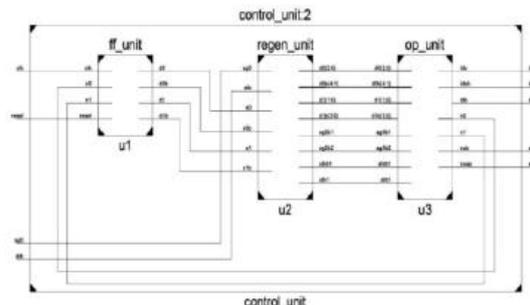


Fig. 9: Block diagram of GCD Control Unit

B. Block Diagram Description:

1) Flip-flop Module

The control unit for GCD processor requires two Flipflops as binary state encoding is used for FSM. In this design reversible edge-triggered D Flip-flop is employed for state transitions [7]. Two D-latches are connected in Master-Slave mode to act as an edge-triggered D Flip-flop.

Reversible D-latch is designed using Feynman and Fredkin gates [8]. RTL schematic of reversible D flip-flop obtained is shown in fig. 10:

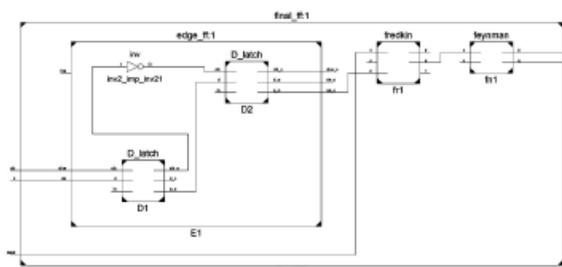


Fig. 10: RTL schematic of Reversible D flip-flop

2) Regeneration Module

To avoid multiple fan-out condition in the design, it is necessary to duplicate signals used for computation of output and next state. The duplication of input signals is achieved using Feynman gates.

3) Output Module

The computation of the outputs and Next-state signals is done using reversible Fredkin gates. The functioning of output signals is driven by the algorithm.

C. Final RTL schematic:

The complete RTL schematic of GCD control unit is shown in fig. 11.

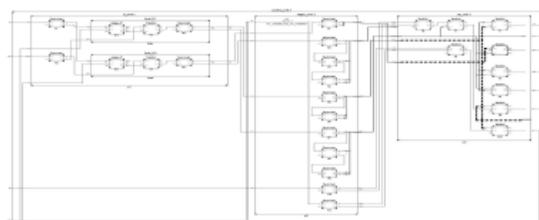


Fig 11: RTL schematic Diagram of GCD Control Unit



D. Speed and power analysis:

Table 3: Comparison of Reversible and Irreversible Control

Parameter (spartan3 xc3s50 family)	Irreversible GCD control unit	Reversible GCD control unit	Percentage improvement for reversible circuit
Speed(Max Clock freq)	434.33MHz	456.09MHz	5.01%
Power	25.02mW	24.19mW	3.31%

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VII. CONCLUSION

In this paper, it can be seen that the performance of digital circuits can be enhanced using reversible gates and have compared 8-bit ripple carry reversible adder with an irreversible adder in terms of speed and power; thereby concluding that reversible designs are faster and power efficient. Furthermore, this concept is extended to combinational circuits such as a Wallace tree multiplier using reversible gates, which were simulated and respective results validate prior inferences. Then a reversible sequential control unit of a GCD processor was designed. Thus, all the designs implemented were compared with their irreversible counterparts, and the speed and power parameters for the reversible designs were observed to have improved significantly.

VIII. APPLICATIONS AND FUTURE SCOPE:

Reversible logic design finds applications in various fields including Quantum computing, Nano-computing, optical computing, Quantum Computing Automata (QCA: study of mathematical objects called Abstract machines and the computational problems that can be solved using them), ultra- low power VLSI designing, Quantum dot cellular etc. The future of computer chips is limited by Moore's law; hence an alternative is to build quantum chips. Our future research topic is designing a new reversible gate and to implement reversible logic into a complete Quantum processor capable of ultra-high speed and infinitesimally low power computing.

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