ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING

National Conference on Advanced Innovation in Engineering and Technology (NCAIET-2015)

Alva's Institute of Engineering and Technology, Moodbidri

Vol. 3, Special Issue 1, April 2015

Design and Implementation of Universal Modulator using Two- Level Pipelined Cordic Structure

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Abstract: Different architectures have been proposed for FPGA implementation of Universal Modulator. The Look up table (LUT) technique is one way of realizing universal modulator. Here the CORDIC is used for efficient realization of Universal Modulator. The coordinate rotation digital computer (CORDIC) algorithm is widely used in various technological fields such as digital signal processing (DSP), biomedical signal processing, robotics, communication systems, image processing etc. Due to ease of simple shift and add operations, the use of CORDIC based systems is increasing drastically. The Universal Modulator is used for realizing Amplitude, Frequency and Phase Modulation. The generation of SIN and COS output values will are tested for a given input angle (θ) value. The universal modulator will be designed around the CORDIC algorithms which can generate all most all digital modulation schemes such as ASK, PSK, FSK**.**

Keywords: Universal Modulator CORDIC, ASK, FSK, PSK, FPGA.

I. INTRODUCTION

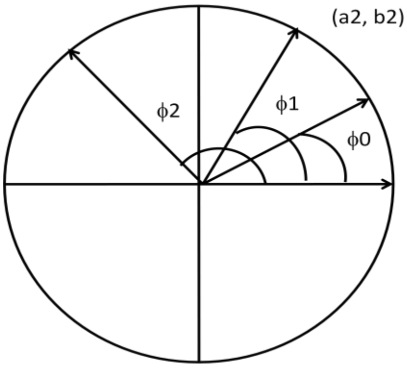
The coordinate rotation digital computer (CORDIC) algorithm is a well-known iterative technique to perform various basic arithmetic operations including the computation of trigonometric functions, vector magnitude estimation, polar to rectangular transformation etc. It is preferred due to its simple shift-add operations, low cost and less complexity. It is possible to generate the carrier directly by using an algorithm called CORDIC . CORDIC algorithm avoids the use of function generator which generates a carrier or different wave forms like sine wave, triangular wave, square wave etc. By using CORDIC algorithm, the digital modulation techniques can also be implemented like ASK, FSK, PSK, and QPSK. A carrier generator is generated by using CORDIC algorithm for digital modulation techniques by avoiding hardware complexity at very less power.

CORDIC may not be the fastest technique to perform these operations, it is attractive due to the simplicity of its hardware implementation, since the same iterative algorithm could be used for all these applications using the basic shift-add operations. Some of the typical approaches for reduced-complexity implementation are focused on minimization of the complexity of scaling operation the basic principle underlying the CORDIC-based computation, and present its iterative algorithm for different operating modes and planar coordinate systems. The objective of this paper is to extend the scheme proposed in [3] for the implementation of CORDIC based universal modulator on Spartan 3E FPGA. Its performance is studied by realizing amplitude, frequency and phase modulation schemes.

This paper is organized in following sections: Section II gives overview of the CORDIC Algorithm. Section III gives the review work. Section IV explains the universal modulator using CORDIC. Section V gives the conclusion.

II. CORDIC ALGORITHM

All of the trigonometric function can be computed or derived from function using vector rotations shown in fig 1. Vector rotation can also be used for polar to rectangular and rectangular to polar conversion, for vector magnitude. The CORDIC algorithm provides an iterative method of performing vector rotations by arbitrary angles using only shifts and adds. . The algorithm, credited to Volder[1], is derived from the general rotation transform:



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$$x' = x\cos\phi - y\sin\phi$$
$$y' = y\cos\phi + x\sin\phi$$

Which rotates a vector in a Cartesian plane by the angle ϕ. These can be rearranged so that:

$$x' = \cos\phi.[x - y\tan\phi]$$
$$y' = \cos\phi.[y - x\tan\phi]$$

If the rotation angles are restricted so that $\tan(\phi) = \pm 2^{-i}$, the multiplication by the tangent term is reduced to simple shift operation.

If the decision at each iteration, i, is which direction to rotate rather than whether or not to rotate, then the $\cos(\delta_i)$ term becomes a constant. The iterative rotation can now be expressed as:

$$x_{i+1} = k_i[x_i - y_i.d_i.2^{-i}]$$
$$y_{i+1} = k_i[y_i - x_i.d_i.2^{-i}]$$

Where

$$k_i = \cos(\tan^{-1}2^{-i}) = \frac{1}{\sqrt{1+2^{-2i}}}$$

and $$d = \pm 1$$

The rotation algorithm has a gain, A_n, of approximately 1.647. the exact gain depends on the number of iterations, and obeys the relation

$$A_n = \prod_n \sqrt{1+2^{-2i}}$$

For rotation mode, the CORDIC equation are:

$$x_{i+1} = x_i - y_i.d_i.2^{-i}$$
$$y_{i+1} = y_i - x_i.d_i.2^{-i}$$
$$z_{i+1} = z_i - d_i.\tan^{-1}(2^{-i})$$

Where

$d_i = -1$ if $z < 0$, $+1$ otherewise.

Which provide the following result:

$$x_n = A_n[x_0\cos z_0 - y_0\sin z_0]$$
$$y_n = A_n[y_0\cos z_0 + x_0\sin z_0]$$
$$z_n = 0$$
$$A = \prod_n \sqrt{1+2^{-2i}}$$

If the angle accumulator is initialized with zero, it will contain the traversed angle at the end of the iteration. In vectoring mode, the CORDIC equation are:

$$x_{i+1} = x_i - y_i.d_i.2^{-i}$$
$$y_{i+1} = y_i - x_i.d_i.2^{-i}$$
$$z_{i+1} = z_i - d_i.\mathrm{tam}^{-1}(2^{-i})$$

Where

$d_i = +1$ if $y < 0$, -1 otherewise.

Then:

$$x_n = A_n\sqrt{{x_0}^2 + {y_0}^2}$$
$$y_n = 0$$
$$z_n = z_0 + \tan^{-1}\left(\frac{y_0}{x_0}\right)$$
$$A_n = \prod_n \sqrt{1+2^{-2i}}$$

For composite rotation angles larger than $\frac{\pi}{2}$, an additional rotation is required. Volder[1] describes an initial rotation $\pm\frac{\pi}{2}$. This gives the correction iteration:

$$x' = -d.y$$
$$y' = d.x$$
$$z' = z + d.\frac{\pi}{2}$$

where

$d_i = +1$ if $y < 0$, -1 otherewise.

III. REVIEW WORK

Mr. J.E. Volder in [1] has proposed the CORDIC Trigonometric Computing Technique the COordinate Rotation DIgital Computer (CORDIC) is a special purpose digital computer for real time computation. In this computer a unique computing technique is employed which is especially suitable for solving the trigonometric relationship. This involved phase coordinate rotation and conversion from rectangular to polar coordinates. In this paper only the trigonometric algorithm used in this computer and instrumentation of this algorithm.

The CORDIC computing technique is especially suitable for use in a special-purpose computer where the majority of the computation involves trigonometric relationship. In general, the ROTATION and VECTORING operations should be considered constant-length routine in which the number of word times per operation is equal to the word length. While not covered in this paper, similar algorithms have been developed for multiplication, division, conversion between binary and mixed radix systems, and extraction of square root, hyperbolic coordinate transformation exponentiation and generation of logarithm. It is believed that similar algorithm based on this fundamental concept of computation could be developed for many other computing requirements.

J. Walther in [2] has proposed a unified algorithm for elementary functions. In this paper they showed that, by varying a few simple parameters it could be used as a single algorithm for unified implementation of a wide range of elementary transcendental function. This function involving logarithm exponential and square roots along with those suggested by [1]Volder. Next, in the year 2009 marks the completion of 50 years of the invention of CORDIC by Jack E. Volder. The CORDIC lies in the fact that by simple shift-add operations. It can perform several computing tasks such as the calculation of trigonometric, hyperbolic and logarithmic functions, real and complex multiplications, division, square-root, solution of linear systems, eigenvalue estimation and many others.

Meher, P.K. et.al in [3]. Has designed a 50 Years of CORDIC: Algorithms, Architectures, and Applications. Year 2009 marks the completion of 50 years of the invention of CORDIC (COordinate Rotation DIgital Computer) by Jack E. Volder. The beauty of CORDIC lies in the fact that by simple shift-add operations, it can

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perform several computing tasks such as the calculation of trigonometric, hyperbolic and logarithmic functions, real and complex multiplications, division, square-root, solution of linear systems, eigenvalue estimation, singular value decomposition, QR factorization and many others. As a consequence, CORDIC has been utilized for applications in diverse areas such as signal and image processing, communication systems, robotics and 3-D graphics apart from general scientific and technical computation. In this article, they gave a brief overview of the key developments in the CORDIC algorithms and architectures along with their potential and upcoming applications.

In the last fifty years, several algorithms and architectures have been developed to speed up the CORDIC by reducing its iteration counts and through its pipelined implementation. Moreover, its applications in several diverse areas including signal processing, image processing, communication, robotics and graphics apart from general scientific and technical computations have been explored. Latency of computation, however, continues to be the major drawback of the CORDIC algorithm, since it does not have efficient algorithms for its parallel implementation. But, CORDIC on the other hand is inherently suitable for pipelined designs, due to its iterative behaviour, and small cycle time compared with the conventional arithmetic. For high-throughput applications, efficient pipelined-architectures with multiple-CORDIC units could be developed to take the advantage of pipeline ability of CORDIC, because the digital hardware is getting cheaper along with the progressive device-scaling. Research on fast implementation of shift-accumulation operation, exploration of new number systems for CORDIC, optimization of CORDIC for constant rotation have scope for further reduction of its latency. Another way to use CORDIC efficiently, is to transform the computational algorithm into independent segments, and to implement the individual segments by different CORDIC processors. With enhancement of its throughput and reduction of latency, it is expected that CORDIC would be useful for many high-speed and real-time applications. The area-delay-accuracy trade-off for different advanced algorithms may be investigated in detail and compared with in future work.

Peter Nilsson in [7] has proposed the complexity reduction in unrolled CORDIC architectures. Here he shows a novel methodology to reduce the complexity in unrolled CORDIC architectures. The methodology is based on eliminating the CORDIC stages starting from the first stage. As an example, a six stage CORDIC is used but the methodology is applicable on CORDICs with an arbitrary number of stages. The paper shows that the complexity can be reduced by 25%.

Naresh V et.al in [8]. Has designed an area efficient multiplexer based CORDIC. In this, the efficacy of this approach is studied for the implementation on FPGA. For this study, both non pipelined and 2 level pipelined CORDIC with 8 stages and using two schemes - one using adders in all the stages and another using multiplexers in the second and third stages. It is found that the nonpipelined and pipelined CORDICs using multiplexer requires 1.6, 1.4 times lower area in Xilinx FPGA and 1.8, 1.6 times lower area than that using only adders. This is achieved without reduction in speed.

IV. UNIVERSAL MODULATOR USING CORDIC

By observing all the authors works, proposes a Universal Modulator. Using the two levels pipelined CORDIC architecture which operates in Rotation mode works as a Universal Modulator. Universal modulator realises the amplitude frequency and phase modulation. The block diagram is basic block of universal modulator.

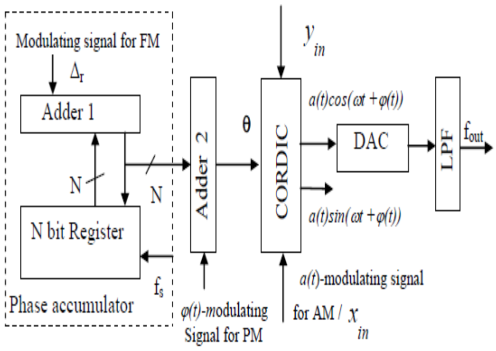

Fig1: Basic block of universal modulator[10]

The various input of the system is used for Amplitude modulation, Frequency modulation and Phase modulation. This universal modulator consist of adders, register, phase accumulator which is used to control the frequency component. Adder provides phase control in the CORDIC. For the system inputs, x_{in} y_{in} for amplitude(AM) realization, Δ_r for frequency(FM) realization and φ(t) for phase(PM) realization. Register used for memory of standard 2GB, which stores the value of the FM adder output and gives the value to add with FM Δ_r as previous value.

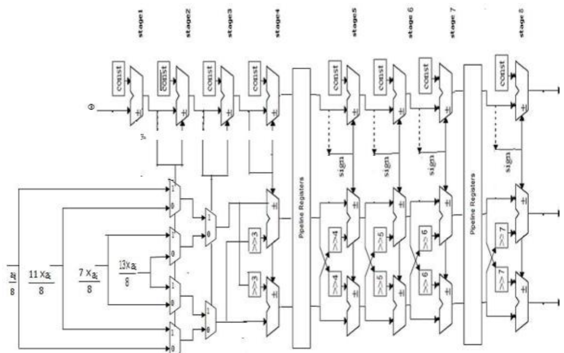

Fig 2: Two- level pipelined CORDIC structure[10]

In this work a pipelined CORDIC of 2 stages of multiplex is proposed for efficient realization of Universal

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Modulator. Its performance is compared with the other CORDIC architecture like, Unrolled CORDIC and MUX based Unpipelined CORDIC.

V. CONCLUSION

All the authors have proposed different type of CORDIC architecture to solve the trigonometric relationship for realization of Universal Modulator. But that proposed technique having some tradeoff between speed and the delay. The aim of pipeline approach for MUX based CORDIC is to obtain sine and cosine of angle with an improved in area and delay.

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