

Comparison Of A Novel Non-Conventional Multi-level Inverter For Different Levels

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Abstract: Multi-level inverters play a key role in present days as the output obtained from it is of high quality as it contains less harmonic distortion and almost similar to sine-wave. Multi-level inverters are used at high power and voltage purposes which are required by the industries, hence the growth of Multi-level inverters. In this paper, a novel non-conventional Multi-level inverter topology is developed with less number of voltage sources and switching devices, and this developed topology is compared for different levels. Asymmetric condition is verified for this proposed novel non-conventional Multi-level inverter topology by using MATLAB SIMULINK software.

Keywords: Multi-level inverter, Novel Non-conventional topology, Asymmetric condition, Comparison, Different levels, MATLABSIMULINK software.

I. INTRODUCTION

Multi-level inverters are used for high power and voltage applications. The output from Multi-level inverter is of stepped waveform almost equal to sine-wave and got good quality. Instead of increasing the ratings of individual switches, the voltage levels are increased in the inverter for obtaining the increase in power ratings. However, a larger number of levels increase the number of devices that must be controlled and the control complexity. There are 3 conventional Multi-level inverters. (i) the neutral point clamped (NPC) or diode clamped multilevel inverter, (ii) the flying capacitor (FC) multilevel inverter and (iii) the cascaded H-bridge (CHB) multilevel inverter [1],[2],[3]. The three conventional Multi-level inverters are shown in fig(1).

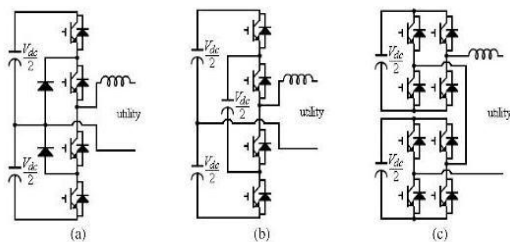


Fig. 1. (a) Diode Clamped Multilevel Inverter (b) Capacitor Clamped Multilevel Inverter (c) Cascaded H-Bridge Multilevel Inverter.

In past years, number of topologies are developed concentrating on various aspects like reducing switching devices, voltage sources etc [4],[5],[6],[7]. In this paper, both the reduction of switching devices and also reduction of voltage sources is concentrated and when compared to conventional model this developed topology has got less number of switching devices and voltage sources for generating a certain levels.

II. PROPOSED TOPOLOGY

A. Seven Level

The circuit configuration for the seven-level inverter is shown in fig (2). For generating a seven-level 2 constant voltage sources ($V_1 = V_{dc}, V_2 = 2V_{dc}$) and 8 switching devices ($S_1, S_2, S_3, S_4, T_1, T_2, T_3, T_4$) are required. S_1-S_4 switches are used as sub-Multi-level inverter and the output from this is positive half-cycles similar to full wave rectifier and this output is fed to switches T_1-T_4 which forms a CHB Multi-level inverter and it changes the polarity of the positive half-cycles to positive and negative half-cycles and produces the required seven-level output. The conduction of switches for different levels is shown in the table (1).

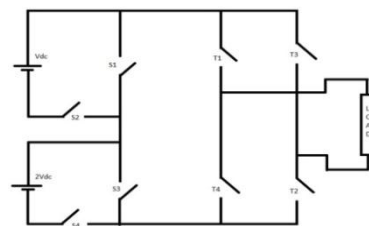


Fig.2. 7-level configuration circuit

Table (1) : 7-level switching table

B. Fifteen-Level

The circuit configuration for the fifteen-level inverter is shown in fig (3). For generating a fifteen-level 3 constant voltage sources ($V_1 = V_{dc}, V_2 = 2V_{dc}, V_3 = 4V_{dc}$) and 10 switching devices ($S_1, S_2, S_3, S_4, S_5, S_6, T_1, T_2, T_3, T_4$) are required. S_1-S_6 switches are used as sub-Multi-level inverter and the output from this is positive half-cycles similar to full wave rectifier and this output is fed to switches T_1-T_4 which forms a CHB Multi-level inverter and it changes the polarity of the positive half-cycles to positive and negative half-cycles and produces the required fifteen-level output. The conduction of switches for different levels is shown in the table (2)

Mode	S1	S2	S3	S4	S5	S6	T1,T2	T3,T4	V0
1	OFF	ON	OFF	ON	OFF	ON	ON	OFF	7vdc
2	ON	OFF	OFF	ON	OFF	ON	ON	OFF	6vdc
3	OFF	ON	ON	OFF	OFF	ON	ON	OFF	5vdc
4	ON	OFF	ON	OFF	OFF	ON	ON	OFF	4vdc
5	OFF	ON	OFF	ON	ON	OFF	ON	OFF	3vdc
6	ON	OFF	OFF	ON	ON	OFF	ON	OFF	2vdc
7	OFF	ON	ON	OFF	ON	OFF	ON	OFF	vdc
8	ON	OFF	ON	OFF	ON	OFF	ON	OFF	0
9	ON	OFF	ON	OFF	ON	OFF	OFF	ON	0
10	OFF	ON	ON	OFF	ON	OFF	OFF	ON	-vdc
11	ON	OFF	OFF	ON	ON	OFF	OFF	ON	-2vdc
12	OFF	ON	OFF	ON	ON	OFF	OFF	ON	-3vdc
13	ON	OFF	ON	OFF	OFF	ON	OFF	ON	-4vdc
14	OFF	ON	ON	OFF	OFF	ON	OFF	ON	-5vdc
15	ON	OFF	OFF	ON	OFF	ON	OFF	ON	-6vdc
16	OFF	ON	OFF	ON	OFF	ON	OFF	ON	-7vdc

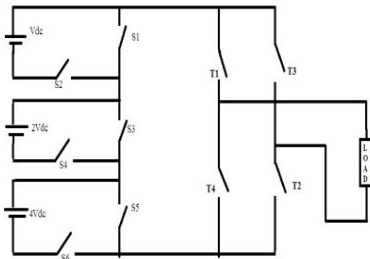


Fig. 3. 15-level configuration circuit

Mode	S1	S2	S3	S4	T1T2	T3T4	Vo
1	OFF	ON	OFF	ON	ON	OFF	3Vdc
2	ON	OFF	OFF	ON	ON	OFF	2Vdc
3	OFF	ON	ON	OFF	ON	OFF	Vdc
4	ON	OFF	ON	OFF	ON	OFF	0
5	ON	OFF	ON	OFF	OFF	ON	0
6	OFF	ON	ON	OFF	OFF	ON	-Vdc
7	ON	OFF	OFF	ON	OFF	ON	-2Vdc
8	OFF	ON	OFF	ON	OFF	ON	-3Vdc

Table (2) : 15-level switching table

III. COMPARISON OF 7 AND 15 LEVELS

In this section, the comparison of those 7 and 15 levels is done. In 7-level 2 dc sources and 8 switches are used, now, just by increasing 1 voltage source, 2 switches and same T1-T4 (CHB) is used for generating 15-level output i.e., 3 voltage sources ($V_1=V_{dc}$, $V_2=2V_{dc}$, $V_3=4V_{dc}$) and 6 switches (S1-S6) and 1 CHB(T1-T4) totally 10 switches are used for generating a 15-level output. Likewise next by increasing 1 voltage source and 2 switches and the same T1-T4 (CHB) i.e., 4 voltage sources ($V_1=V_{dc}$, $V_2=2V_{dc}$, $V_3=4V_{dc}$, $V_4=8V_{dc}$) and 8 switches (S1-S8) and 1 CHB(T1-T4) totally 12 switches are used for generating the 31-level. Similarly, further levels can be generated just by increasing 1 voltage source and 2 switches in the previous level circuit configuration. On comparing fig (2) and fig(3) it is clearly shown, and the working principle is same and the conduction of the switches for different levels for both 7 and 15 levels is shown in table(1) and table(2).

IV. SIMULATION RESULTS

The simulation circuit for the 7-level and 15-level are shown in fig(4) and fig(5). Both levels are simulated using MATLABSIMULINK software only. All the blocks used for simulation are obtained from commonly used blocks and sim power systems obtained from simulink library. The output obtained from sub Multi-level inverter is of positive pulses i.e., similar to full wave rectifier is shown

in fig (6) and fig(7) for 7-level and 15 –level. The output of sub Multi-level inverter is fed to CHB (T1-T4) and thus CHB changes the polarity of those positive pulses to both positive and negative and thus the output obtained is in the form of step waveform and almost equivalent to sine-wave . The output of 7-level and 15-level are shown in fig(8) and fig(9).

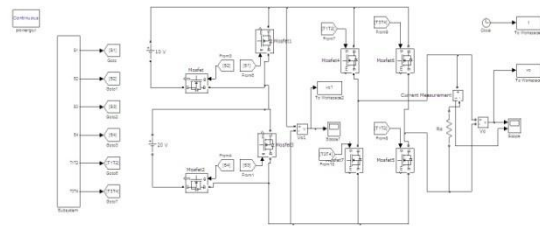


Fig.4. 7-level simulation circuit

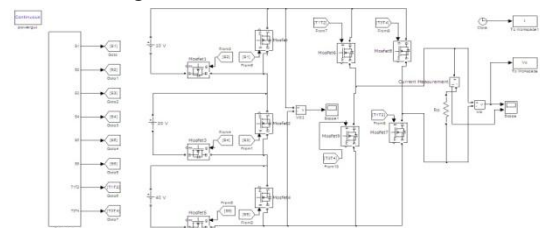


Fig.5. 15-level simulation circuit

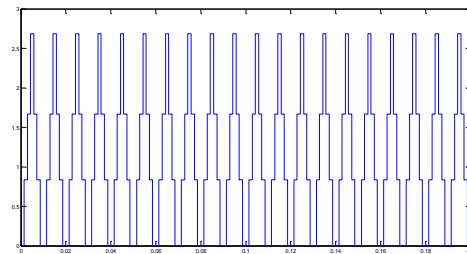


Fig. 6.7-level positive cycles(output of sub Multi-level inverter).

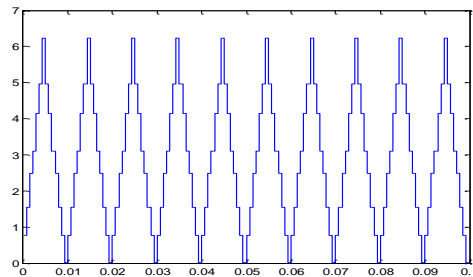
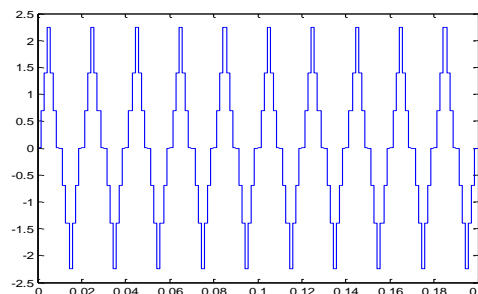


Fig. 7.15-level positive cycles(output of sub Multi-level inverter).



level output waveform

Fig. 8 . 7-

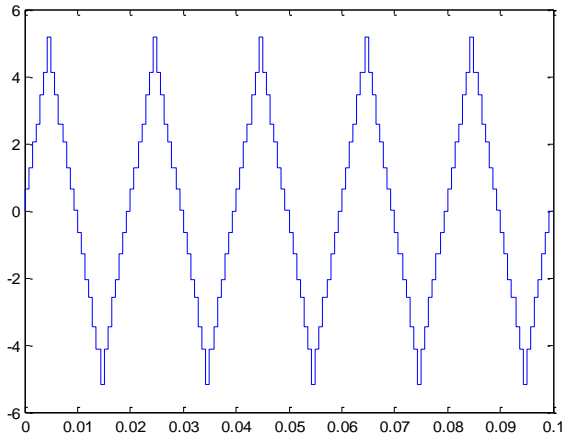


Fig. 9 . 15-level output waveform

V. CONCLUSION

In this paper, a novel non-conventional Multi-level inverter topology is developed with less number of switching devices and voltage sources. Later level topologies are also developed for the present developed topology and the link for generating the further large level topologies is also described. Comparison is done among those different level topologies and their simulation results are produced using MATLABSIMULINK software along with their principle of operation. Thus the reduction of both voltage sources and switching devices for higher levels is concentrated in the present topology of the Multi-level inverter than those of the conventional type of Multi-level inverters.

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BIOGRAPHIES

Sadhu Renuka received B. Tech degree in Electrical and Electronics Engineering from G. Pulla Reddy Engineering college , SKU, Anantapur in the year 2013. She is currently pursuing M.Tech in G. Pulla- Reddy Engineering College, JNTUA, Kurnool. Her research interests include Electrical Power Converters.

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