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Minimization of leakage current through horizontal step doping in SOI MOSFETs

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Abstract: As technology scales, sub-threshold leakage currents grow exponentially and become an increasingly large component of total power dissipation. To improve performance of the MOSFETs, doping profile of channel is changed. In this paper, we present comparison of uniform doping (UD), horizontal high source side doping (HHSS) &horizontal high drain side doping (HHDS) and draw the various characteristics i.e. channel electric field, surface potential & sub threshold leakage current .our results show that the horizontal high source sidedoping exhibit excellent properties not only higher mobility but also hot electron degradation improvement and better reliability. Therefore, refer to the results, horizontal high source side doping structure has superior performances in comparison with uniform and horizontal high drain side doping (HHDS). All the device simulations are performed using SILVACO Atlas device simulator.

Keywords: Uniform doping (UD), Horizontal high source side doping (HHSS), Horizontal high drain side doping (HHDS), short channel effects (SCEs), ATLAS.

I. INTRODUCTION

As scaling of MOSFET dimensions decreased channel lengths under 50 nm, high doping concentration or thinner gate oxide hasto be used in order to achieve higher drain current. But, the high doping concentration reduces mobility due to higher Coulomb scattering rates Also, the reduction of the silicon-dioxide gate dielectric thickness for drive current improvement leads to increase direct tunneling gate leakage current and standby power consumption. Furthermore it increases concerns regarding the gateoxide reliability. Therefore, new structure horizontal high source side doping (HHSS) is introduced to improve device performance by enhancing doping concentration in channel region [1].

SOI STRUCTURE: It refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrate, to remove parasitic capacitances, and problem of latch-up and thereby improve the performance of the devices .Fig. 1.1 shows ultra-thin body SOI MOSFETs.

The choice of insulator depends largely on intended application, with sapphire being used for high-performance radio frequency (RF) and radiation-sensitive applications, and silicon dioxide for diminished SCEs [3]in microelectronics devices. They are attractive devices for low-power high-speed very large scale integration (VLSI)[7] applications because of small parasitic capacitances. Young analyzed the SCEs[3] using a device simulator, and concluded that SCEs are well suppressed in thin-film SOI MOSFET's when compared to bulk MOSFETs. In general, it is believed that thin-film SOI MOSFETs has a higher immunity to SCEs when compared with bulk MOSFETs [1].

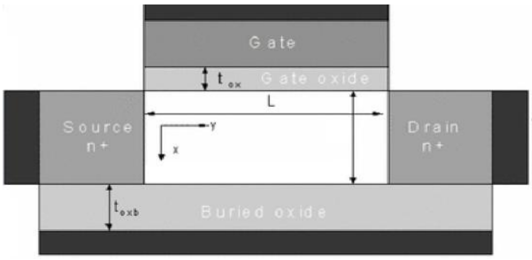

Fig. 1.1 Schematic diagram of an UTB-SOI MOSFET

II. PREVIOUS WORK

In this paper, the unique features exhibited by a novel nanoscaleSiGe-on-insulator metal-oxide-semiconductor field-effect transistor (MOSFET) with modified channel band energy.

The key idea in this work is to modify the band energy in the channel for improving electrical performances. Graded Ge composition profile is employed in the channel that leads to call the proposed structure as GC-SGOI structure. Using two-dimensional two-carrier simulation [10]we demonstrate that the GC-SGOI structure has higher saturation velocity in comparison with stepped (SC-SGOI) and uniform (UC-SGOI) germanium composition due to the high conduction and valence bands slopes by using graded Ge composition profile.

Also, our results show that the GC-SGOI exhibit excellent properties not only higher mobility, drain current and saturation velocity but also hot electron degradation improvement and better reli-ability[2]

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III. PROPOSED METHODOLOGY

This chapter simulates the various charecteristics of HHDS SOI MOSFETs through ATLASsimulator. It may be noted that the ATLASsimulator measures all the result of channel potential with respect to average Fermi potential of the intrinsic silicon.

The drift-diffusion (DD) model has been used instead of the energy balance (EB) model, since DD model can predict I-V characteristics of short-channel MOS devices more realistically than the EB model. The source/Drain to body junctions are assumed to be abrupt with doping concentration of the source/drain regions $N_{DS} = 10^{20}$ cm^{-3}. The values of all perameters used in simulation of HHDS SOI-MOSFETs is given in Table No. 1.2.

Parameter	Value
Permittivity of free space (ε_0)	$8.85418782 \times 10^{-12}$ m^{-3} kg^{-1} s^4 A^2
Permittivity of Si (ε_{si})	$11.2\varepsilon_0$
permittivity of Si oxide (ε_{ox})	$3.9\varepsilon_{ox}$
Metal workfuction (ϕ_M)	4.3ev
Silicon energy band gap(E_{gsi})	1.08ev
Silicon electron affinity(X_{si})	4.17ev
Channel length (L)	40 nm
Channel thickness(t_{si})	10 nm
Gate oxide thickness(t_{ox})	2 nm
Buride oxide thickness (t_{oxb})	100 nm
Source/Drain doping(N_D/NA)	10^{20} atom/cm^3

Table No. 1.2

Structure of uniform doping:-In uniform doping, the whole channel is doped by same element,p-type silicon channel impurity with a uniform doping level of1×10^{17}cm^{3}is utilized..Fig 1.3shows structure of uniform doping.

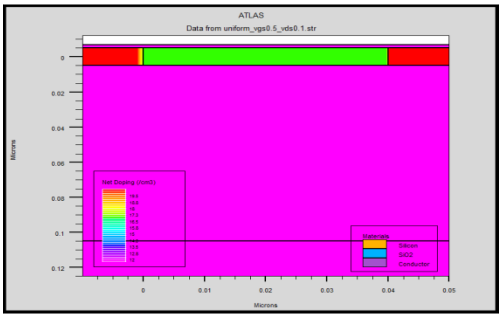

Fig 1.3Structure of Uniform doping

Horizontal high step doping at drain side (HHDS):In this structure, the doping of channel is done in four steps, each having a length of 10nm.the doping is maximum at drainside.Doping is linearly graded from 1×10^{15}cm^{3}to 1×10^{19}cm^3 Fig 1.4 shows structure of horizontal highdrain side doping (HHDS).

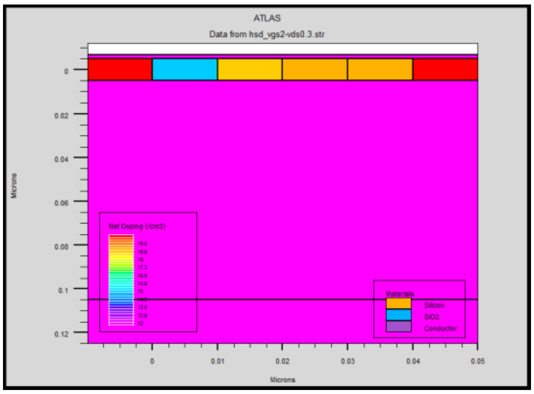

Fig 1.4Structure of Horizontal high step doping at drain side(HHDS)

Horizontal high step doping at source side(HHSS): In this structure, the doping of channel is done in four steps, each having a length of 10nm.the doping is maximum at source side. Doping is linearly graded from1×10^{19}cm^{3}to 1×10^{15}cm^{3}fig 1.5 shows structure of Horizontal high step doping at source side(HHSS).

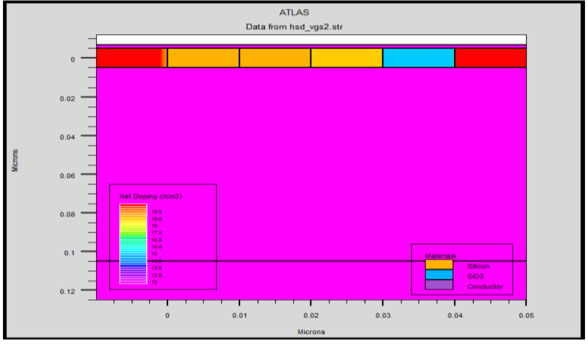

Fig 1.5Structure of Horizontal high step doping at source side (HHSS)

Doping distribution profile: We have compared the uniform structure, HHSS&HHDS with equivalent parametersexcept doping distribution profile. Fig 1.6 shows the channel doping profile along channel length in uniform doping, horizontal high source side doping & horizontal high drain side doping.

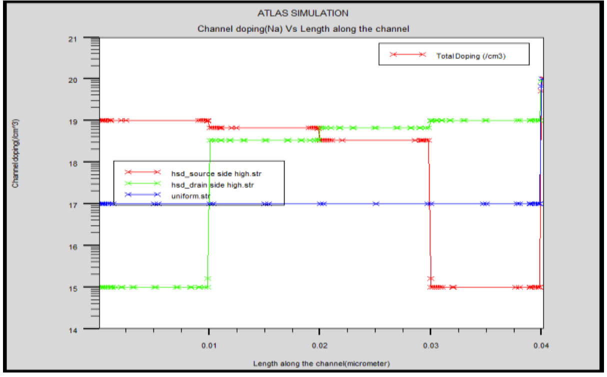

Fig 1.6 Doping distribution profile in the channel for theuniform structure, HHSS& HHDS

IV. RESULT AND DISCUSSION

The Simulation results obtained from ATLAS device simulator are Surface potential, electric field along the channel length.

Surface potential: In order to have better physical insight of the structures performance horizontal high source side doping ,high drain side doping and uniform doping , we simulated variation of thepotential barrierheight alongthe AA′ cutline locatedat5nmfromthesurfaceof thestructure.

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As it is clear from thefigure, the potentialbarrierheightvariation in horizontal high source side dopingissignificantlymorethanhigh drain side doping and uniform doping. This figure 2.1 illustrates the minimum surface potential shifts downward with increases in horizontal high source side doping gradients in channel region.

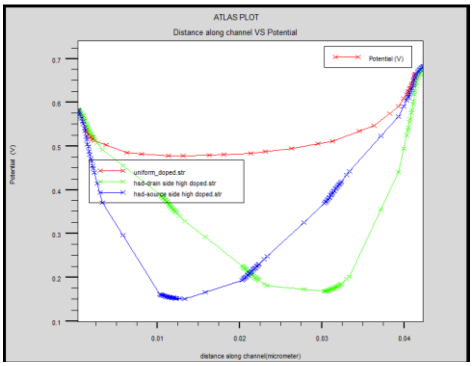

Fig 2.1 variation of surface potential versus position in channel for the uniform doping, HHSS &HHDS structures along the AA'cutline at V_G=0.2 V and V_D=0.1 V.

Channel Electric field: Fig.2.2 shows the electricfield of the proposed, uniform doping, HHSS &HHDSstructures along the lateral position atV_G=0.2 V andV_D=0.1 V. The electricfield enlargement near the source junction leads to its peakreduction near the drain region at afixed drain voltage [8, 9]. So, when electricfield enhance near the source region, device carriers get accelerated which causes saturation velocity, carriers mobility and drain current growth. On the other hand, hot carriers are generated near the drain region due to the electric field peak which accelerates them for injection into the gate oxide. So, because of theelectricfield peak value reduction near the drain region, the electron temperature, gate and substrate currents of the proposed structure get decreased[8,9]The built-in electric field improves the on current of device that accelerates the channel carriers and easestheir transportation.

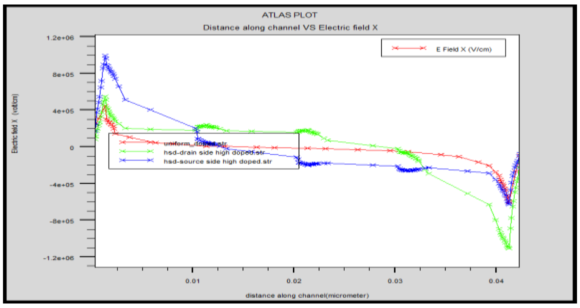

Fig: 2.2 Electric field distribution profiles versus position in channel for the uniform doping, HHSS &HHDS structures along the AA'cutline at V_G=0.2 V and V_D=0.1 V.

Electron velocity: Fig: 2.3 shows variation of Electron velocity along the channel length for different channel doping in uniform doping, Horizontal high source side doping (HHSS)&Horizontal high drain side doping(HHDS) . At lower horizontal effective electricfield, the peak value of the mobility is extracted.

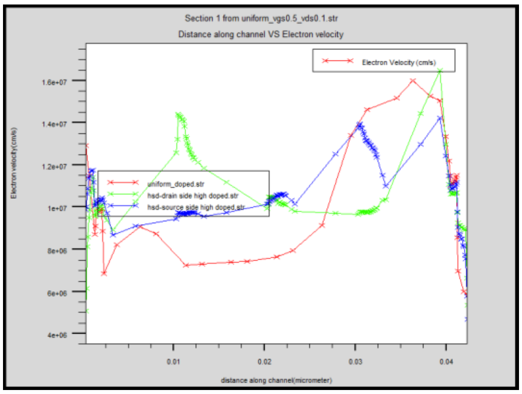

Fig: 2.3 Variation of Electronvelocity along the channel length for different channel doping

V.CONCLUSION

We have introduced comparison of uniform doping (UD),horizontal high source side doping(HHSS) & horizontal high drain side doping(HHDS) and draw the various characteristics i.e. channel electric field ,surface potential & electron velocity. From above results it is clear that short channel effects is also reduced .The drain current is high at horizontal high drain side doping(HHDS) than horizontal high source side doping(HHDS).Therefore the good properties and superior performance of the novel structure persuade us to use it in VLSI low power integrated circuits.

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REFERENCES

[1] MortezaRahimian, and Ali A. Orouji, *"A novel deep submicron SiGe-on-insulator (SGOI) MOSFET with modified channel band energy for electrical performance improvement,"* Current Applied Physics 13,pp 779 - 784, 2013.

[2] Ali A. Orouji andMortezaRahimian, *"Leakage current reduction in nanoscale fully-depleted SOI MOSFETs with modified current mechanism,"*Current Applied Physics 12 ,pp 1366 – 1371, 2012.

[3] K.KONRAD YOUNG, *"Short-Channel Effect in Fully Depleted SOI MOSFET's,"*IEEE TRANSACTIONS ON ELECTRON DEVICES. VOL 36. NO 2.,pp 399-402,1989.

[4] AnuragChaudhry, M. Jagadesh Kumar,*" Investigation of the novel attributes of a fully depleted dual-material gate SOI MOSFET"*, IEEE Trans. Electron Dev. 51(9),pp. 1463-1467, 2004.

[5] UditMonga,Tor A. Fjeldly, *"Compact Subthreshold Current Modeling of Short-Channel Nanoscale Double-Gate MOSFET,"* IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 56, NO. 7, pp.1533-1537, 2009.

[6] V. De ,S. Borkar, *"Technology and design challenges for low power and high performance,"* Proc. Int. Symp.Low Power Electron. Des,

[7] Fundamentals of Modern VLSI Devices. New York: Cambridge Univ. Press, ch. 3, pp.120–128, 1998.

[8] H. Elahipanah,Ali A. Orouji,*"A novel step-doping fully-depleted silicon-on-insulator metal oxide semiconductorfield-effect transistor for reliable deepsub-micron devices"*,Jpn. J. Appl. Phys. 48 (8), pp. 114503-114508, 2009.

[9] H. Shin , S. Lee,*"An 0.1-m asymmetric halo by large-angle-tilt implant (AHLATI)MOSFET for high performance and reliability"*, IEEE Trans. Electron Device 46(4) pp.820-822, 1991.

[10] J. Werne, M. Oehme, E. Kasper, J. Schulze,*" Influence of modulation doping tothe mobility of two-dimensional electron gases in Si/SiGe, Thin Solid Films"*pp. 234-236, 2010.

BIOGRAPHY

Priyanka Parmar received the B.E degree in Electronics & Communication from Bansal Institute of Science& Technology Bhopal, India. She is currently pursuing her M.Tech in VLSI Design from Shri Ram College of Eng. & Management, Banmore, India. Her current research interests include digital electronics, microelectronic

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