

Anti-Windup PID Based Wind Generation with Power Smoothing Elements

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Abstract: This paper proposes a capacitor clamped multi level inverter anti wind up wind power generation system with power smoothing elements. This technology will place voltage of the capacitor in defined range by replacing with super capacitor. In this paper An Anti wind controller is inserted to overcome the physical limitations of wind turbines. This anti wind up controller uses mainly a pid controller to saturate the output of equipment. A space vector modulation method is proposed in this paper to reduce harmonic distortion caused by the super capacitor in capacitor clamped inverters. Implemented clearly shown in paper. Proposed circuit is analyzed by simulation MATLAB/SIMULINK.

Keywords: flying capacitor, grid, anti wind up, PID Controller

I.INTRODUCTION

In classical power systems, large power generation plants placed at adequate geographical places generates high amount of the power, which is then transmitted towards large power utilizing centers over very long distance transmission lines. The designed system control centers monitor and control the power unit continuously to ensure the power quality, namely the frequency and the voltage. However, now the total power systems is changing, a huge number of dispersed generation (DG) units, including both conventional and non-conventional sources such as wind , wave generators, photovoltaic (PV) generators, tiny hydro, fuel cells and gas/steam power Combined Heat and Power (CHP) stations, are developed [1]-[2] and installed.

A wide-spread use of conventional energy sources in distributed networks and a more penetration level will be seen in the future many places. E.g. Denmark has a much penetration (> 20%) of wind energy sources in major areas of the countries and now a days 18% of the entire electrical power consumption is compensated by wind energy. The key advantages of renewable energy sources are the elimination of hazardous emissions and inexhaustible resources of the primary energy. However, the key disadvantage, apart from the costs, e.g. Photovoltaic, is the best uncontrollability.

The availability of renewable energy sources has robust daily and seasonal patterns and the power requirement by the consumers are having a very different characteristics. Therefore, it is highly complex to operate a power system installation with renewable generation units due to the

characteristic differences and the high uncertain in the available of the renewable sources. The wind turbine technology is best emerging renewable energy technologies. It started in the 1980's with a tens of kW production power to today with MW range wind turbines that are installed.

This also means that wind power production at beginning did not have any impact on the power transmission control but now because of their size they will have to play an active role in the grid. The technology is using in the wind turbines was in the initial variations on a squirrel-cage induction generator connected to the grid. By that power VAR in the wind turbines are almost transferred to the electrical power grid. Furthermore there is uncontrolled of the active and reactive power, which are typically important control the parameters for regulation the frequency and the voltage.

As the range of the turbines increases those control parameters are become more important and it is very necessary to introduce power electronics [3] as to interface between the wind generation and grid. The power electronics is changing the basic characteristics of the wind generation from being an energy source to be an active power sources.

II.SUPER CAPACITOR

The super capacitor, has another name called *ultra capacitor* or *double-layer capacitor*, It differs from a conventional capacitor in that it had a very high

capacitance. A capacitor is to store energy by meaning of a static charge as opposition of an electrochemical reaction. Application of a voltage differential on the +ve and +ve plates will charge the capacitor. This is similar to the building of a electrical charge when walking on a mat. Touching a object releases energy through the finger.

We group capacitors into three types and the basic is the *electrostatic capacitor*, using a dry separator. This capacitor has a low capacitance and is used to purify signals and tune radio frequencies. The size ranges from a pico-farad (pf) to microfarad (uF). The second type is the *electrolytic capacitor*, which is used in power filtering, buffer and couple. Indicated ratings in microfarads (uF), this capacitor had several times the storage capacity of the electrostatic capacitor. The third one is the *super capacitor*, rated in farads, which is in thousands of times higher than normal electrolytic capacitor. The super capacitor is unique for energy storage undergoes frequent charge and discharge cycles at huge current and short durations.

The modern supercapacitor is not belongs a batteries but crosses the boundaries into battery technologies by using special type of electrodes and electrolyte. Several types of electrodes have been used and we focus only on the double-layer capacitor (DLC) concept. It is a carbon-based, has an organic electrolyte that is flexible to manufacture and is the most common system in using today.

III PID ANTIWINDUP

There are so many different ways to protect from windup. Tracking is a easy method which is explained in the fig.1 below. The system has an extra feedback path around the integrator. The signal is difference between the nominal controller of output voltage and the saturated controller output.

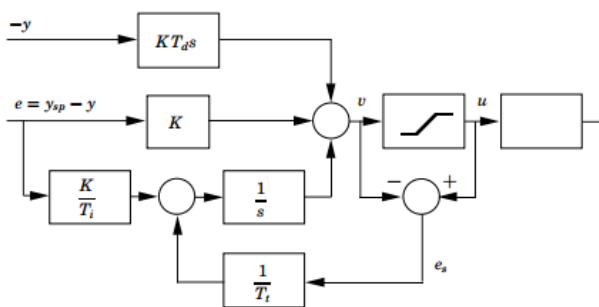


Fig.1 Anti windup system block diagram

The signal is connected to the input of the integrator through gain $1/T_t$. The signal is zero if there is no saturation. Under these bases it don't have any effect on the integrator. When the actuator saturates, signal is widely different from zero and it will try to flow through the integrator output to value that such that the signal is near to the saturation limit. Here are some of exercises that shows the effect of wind-up protection.

- The process transfer function is shown as $P(s) = 1/s$. arrange the tracking time $T_t = 1$ and observe differences in behavior of closed loop with anti windup and a linear PI controller .
- PB Anti-windup, investigates proportional band. Compare to the proportional band for linear controller PB based Windup. Change scales so that transient is much visible. Investigate how process output, the controller the output and integral, and proportional band change with the changing tracker time constant T_t . Compared with controller without any protection windup which correspond to a very large value of T_t .

IV. PROPOSED SYSTEMS

The first step of this analysis is the definition of possible voltage levels in a capacitor-clamped three-level inverter. The line-to-ground voltage of each leg of the inverter can have maximum of four voltage levels. These four voltage levels, corresponding gate signals. The other two legs also follow the same pattern. If super capacitor voltages are balanced, the second and third voltage levels (V_{scA} and $V_{dc} - V_{scA}$) become equal, and hence, the total number of discrete voltage levels get reduced to three (0, $V_{dc}/2$, and V_{dc}). In this particular situation, the switching states "1" and "2" produce the same line-to-ground voltage, i.e., $v_{ag} = V_{dc}/2$. Therefore, these two states are called redundant states. Under this balanced condition, the proposed system acts as a three-level inverter. The corresponding space vector distribution is shown in Fig. 2(a). However, due to overlapping, only 19 discrete vectors are visible in Fig. 2

$$\begin{bmatrix} V_{as} \\ V_{bs} \\ V_{cs} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} V_{ds} \\ V_{qs} \\ 0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_{as} \\ V_{bs} \\ V_{cs} \end{bmatrix} \quad (2)$$

If super capacitor voltages are reduced to one-third of the dc link voltage, each leg of the inverter can produce four

different voltage levels (0, $V_{dc}/3$, $2V_{dc}/3$, and V_{dc}). Therefore, in this case, the same system operates as a four-level inverter with the space vector distribution shown in Fig.2 (b). if super capacitor voltages are increased to two-thirds of the dc-link voltage, each leg of the inverter again produces four different voltage levels (0, $V_{dc}/3$, $2V_{dc}/3$, and V_{dc}). Therefore, the system operates as a four-level inverter in this case too with the space vector distribution shown in Fig 2(c).

Even though this diagram looks very similar to Fig. 2(b), positions of some vectors are interchanged. In the proposed system, the lower limit for super capacitor voltages is kept at $V_{dc}/3$. The space vector diagram shown in Fig. 2(b) corresponds to this situation. Similarly, super capacitor voltages are upper bounded to $2V_{dc}/3$. The corresponding space vector distribution is shown in Fig.2(c). As super capacitor voltages are increased from the lower limit, the innermost hexagon, shown in Fig. 2(b), expands, while the other inner hexagon shrinks. When super capacitor voltages reach $V_{dc}/2$, both inner hexagons get overlapped as shown in Fig. 2(a). Further increase of super capacitor voltage would cause expansion and shrinkage of inner hexagons which eventually end up as in Fig 2(c). For the simplicity of analysis and modulation, space vectors of the proposed flying-capacitor inverter system are classified into nine groups, as in Table II. Out of these nine groups, the last group, named as “Rest,” is not used in the proposed modulation method due to the complexity of corresponding vector patterns.

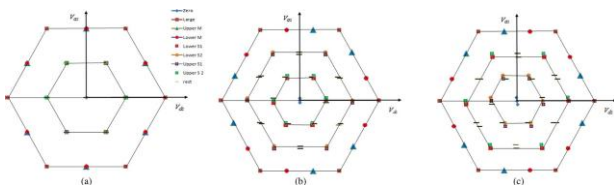


Fig.2 Space vector distribution at different supercapacitor voltage conditions. (a) $V_{sca} = V_{scb} = V_{scc} = V_{dc}/2$. (b) $V_{sca} = 0.33V_{dc}$, $V_{scb} = 0.31V_{dc}$, and $V_{scc} = 0.35V_{dc}$. (c) $V_{sca} = 0.66V_{dc}$, $V_{scb} = 0.64V_{dc}$, and $V_{scc} = 0.68V_{dc}$

TABLE II
VECTOR CLASSIFICATION

Large	Upper medium	Lower medium	Upper Small1	Upper Small 2
003 030	023 032	013 031	113 131	223 232
033 300	203 230	103 130	133 311	233 322
303 330	302 320	301 310	313 331	323 332
Lower Small 1	Lower Small 2	zero	Rest	
001 010	002 020	000 111	012 021 102 112 120	
011 100	022 200	222 333	121 122 123 132 201	
101 110	202 220		210 211 212 213 221	
			231 312 321	

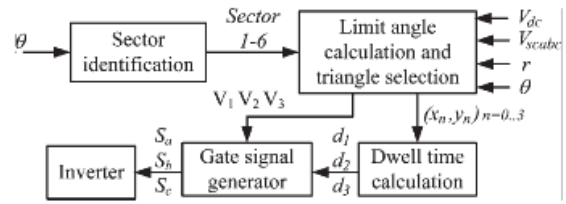


Fig. 3. Simplified block diagram of the proposed SVM technique

V MODULATION STRATEGY

As mentioned in previous sections, imbalanced and unequal capacitor voltages are unavoidable in the proposed system. They use low-capacity (compared to super capacitors) electrolytic capacitors, and therefore, voltage balancing and regulation are possible within a short period of time with the use of advanced balancing techniques. However, due to the high capacity, super capacitors used in the proposed system take long time to change their voltages, and therefore, unequal and unbalanced capacitor voltage conditions can remain for a longtime. The aforementioned modulation strategies are not suitable for this scenario, and therefore, this paper presents a suitable SVM technique which can produce undistorted currents even under unbalanced and unequal voltage conditions. A simplified block diagram of the proposed SVM technique is illustrated in Fig. 3. The amplitude r and the angle θ of the reference voltage vector are calculated using (3) and (4). The currently serving

TABLE III
SECTOR SELECTION CRITERIA

Angle, θ (deg)	$0 \leq \theta < 60$	$60 \leq \theta < 120$	$120 \leq \theta < 180$	$180 \leq \theta < 240$	$240 \leq \theta < 300$	$300 \leq \theta < 360$
Sector	1	2	3	4	5	6

sector of the space vector diagram is derived from the phase angle based on the selection criterion given in Table III

$$R = \sqrt{v_d^{*2} + v_q^{*2}} \quad (3)$$

$$\Theta = \tan^{-1} \left(\frac{v_q^*}{v_d^*} \right) + \theta_{grid} \quad (4)$$

where v^*d and v^*q are d - q -axis components of the reference voltage vector. θ_{grid} is the angle of grid voltage vector.

two limit angles (θ_1 and θ_2) are related to the triangles formed with lower small 1 and upper small 2 vectors as shown in Fig. 4(a), whereas the other two limit angles (θ_3 and θ_4) are associated with the triangles formed with lower small 2 and upper small 1 vectors as shown in Fig. 4(b). For the simplicity of subsequent calculations, dc-side voltages are transformed into two variables x and y using (3). These two values are directly related to the sides of

triangles as marked in Fig. 4. Limit angles are calculated using (7)–(14) where α is an intermediate variable

$$X = \frac{2}{3}(V_{dc} - V_{sc}) \quad y = \frac{2}{3}V_{sc} \quad (5)$$

$$\alpha = \sin^{-1} \left(\frac{\sqrt{3y}}{2\sqrt{(x+y)^2 - 3xy}} \right) \quad (6)$$

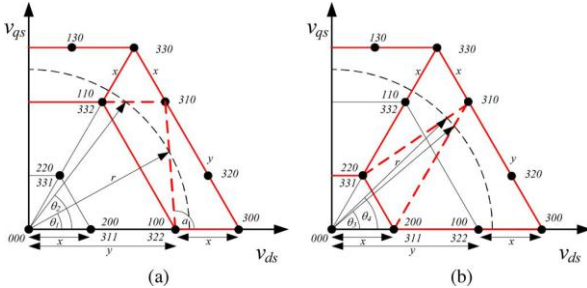


Fig. 4. Limit angles for the sector 1. (a) Limit angles for triangles formed with lower small 1 and upper small 2 vectors. (b) Limit angles for triangles formed with lower small 2 and upper small 1 vectors

TABLE IV
LIMIT ANGLES FOR SECTORS 1–6

Sector	θ_1^*	θ_2^*	θ_3^*	θ_4^*
1	θ_1	θ_2	θ_3	θ_4
2	$2\pi/3 - \theta_2$	$2\pi/3 - \theta_1$	$2\pi/3 - \theta_4$	$2\pi/3 - \theta_3$
3	$2\pi/3 + \theta_1$	$2\pi/3 + \theta_2$	$2\pi/3 + \theta_3$	$2\pi/3 + \theta_4$
4	$4\pi/3 - \theta_2$	$4\pi/3 - \theta_1$	$4\pi/3 - \theta_4$	$4\pi/3 - \theta_3$
5	$4\pi/3 + \theta_1$	$4\pi/3 + \theta_2$	$4\pi/3 + \theta_3$	$4\pi/3 + \theta_4$
6	$2\pi - \theta_2$	$2\pi - \theta_1$	$2\pi - \theta_4$	$2\pi - \theta_3$

$$\theta_1 = \alpha - \sin^{-1} \left(\frac{\sqrt{3y}}{2\sqrt{(x+y)^2 - 3xy}} \right) \quad (7)$$

$$\theta_2 = \sin^{-1} \left(\frac{\sqrt{3y}}{2r} \right) \quad (8)$$

$$\theta_3 = \frac{\pi}{3} - \sin^{-1} \left(\frac{\sqrt{3x}}{2r} \right) \quad (9)$$

$$\theta_4 = \alpha - \frac{\pi}{3} - \sin^{-1} \left(\frac{x}{r} \sin \left(\alpha - \frac{2\pi}{3} \right) \right) \quad (10)$$

$$\theta_5 = \frac{\pi}{3} - \theta_1 \quad (11)$$

$$\theta_6 = \frac{\pi}{3} - \theta_2 \quad (12)$$

$$\theta_7 = \frac{\pi}{3} - \theta_3 \quad (13)$$

$$\theta_8 = \frac{\pi}{3} - \theta_4 \quad (14)$$

The limit angles given in (7)–(14) are valid only for the lower medium vector “310.” The corresponding limit angles for the other medium vector “320” can be derived from these values with the help of (11)–(14). All these limit angles are valid only for the sector 1. Limit angles for other sectors can be derived from these angles with the help of Table IV. Once the limit angles are calculated, the triangle and corresponding three vectors can easily be derived.

IV. SUPERCAPACITOR VOLTAGE EQUALIZATION

The proposed super capacitor voltage equalization method is, based on redundant state selection. Overlapping small vectors, shown in Fig. 2, provide these redundancies. For example, small vectors (100, 322) and (200, 311), shown in Fig. 4, are redundant vector pairs attached to the sector 1. Similarly, there are ten more redundant vector pairs attached to the other five sectors. Half of these redundant vector pairs contribute to super capacitor charging, while the other half tend to discharge super capacitors. In other words, vectors on the middle hexagon, shown in Fig. 4, discharge super capacitors, while the vectors on the inner most hexagon charge super capacitors. In order to explain this phenomenon in detail, four equivalent circuits, corresponding to the aforementioned two vector pairs, are shown in Fig. 6. By looking at the current direction of the a -phase in Fig. 6(a), it

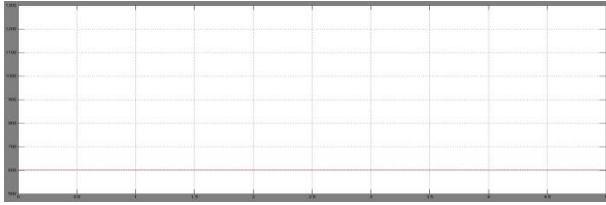
TABLE V
LOOKUP TABLE FOR SMALL VECTOR SELECTION

Sector		1	2	3	4	5	6	
Phase with priority		a	c	b	a	c	b	
Most deviated super capacitor	C_{sc_a}	Charge	20	22	02	13	11	20
		Discharge	0	0	0	3	3	2
	C_{sc_b}	Charge	10	11	23	23	22	10
		Discharge	0	0	2	3	3	1
	C_{sc_c}	Charge	31	22	02	02	11	31
		Discharge	1	0	0	2	3	3
C_{sc_a}	Charge	32	33	02	01	22	32	
	Discharge	2	2	0	1	3	3	
C_{sc_b}	Charge	31	33	13	02	00	20	
	Discharge	1	1	1	2	2	2	
C_{sc_c}	Charge	32	33	23	01	00	10	
	Discharge	2	2	2	1	1	1	

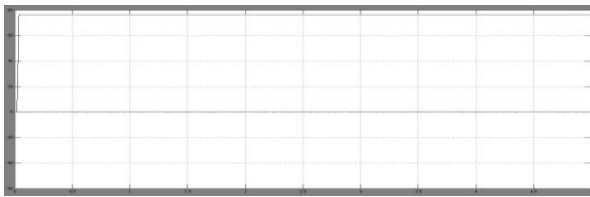
can be deduced that the super capacitor attached to leg “a” gets discharged at the small vector “100.” Similarly, the small vector “322” discharges the other two super capacitors. Therefore, with the proper combination of these two small vectors, discharging rates of super capacitors can be controlled in sector 1. The equivalent circuit in Fig. 6(c) corresponds to the small vector “200” which is on the innermost hexagon shown in Fig. 4. This vector charges the super capacitor attached to the leg “a” of the inverter. Moreover, the other vector of the pair, i.e., “311,” charges the other two supercapacitors as shown in Fig. 6(d). This indicates that the increased use of the small vector “200” charges the super capacitor C_{sca} at a higher rate than that of the other two. The opposite of this happens if the vector “311” is used. The proposed super capacitor voltage equalization method is based on this methodology.

VI.SIMULATION RESULTS

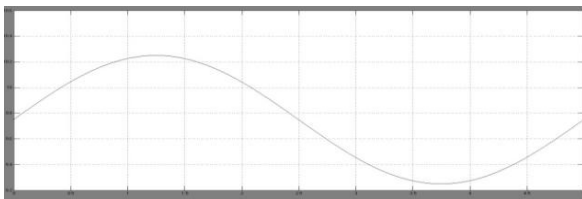
The performance of the proposed super capacitor direct integration scheme has been tested using computer simulations on MATLAB/Simulink platform.



(a)



(b)



(c)

Fig.9 (a) super capacitor voltages(Time Vs V). (b) $d-q$ -axis components of the inverter output currents(Time Vs Amps).(c) Control signal for charge/discharge vector selection(Time Vs constant).

The above results shows in fig 9(a) the variation in capacitor voltages ,with respect to wind speed which will in between 1 unit variation with 10 w/s. Fig9(b) $d-q$ currents of generator variation in generator currents aswell as variation in control signal for charge vector selection.

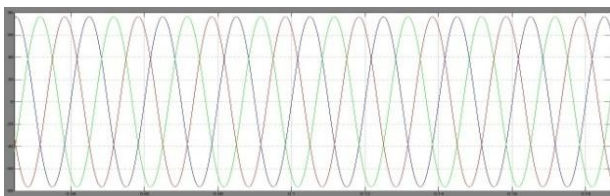


Fig.10 Inverter output current in the balanced condition (Amps Vs Time)

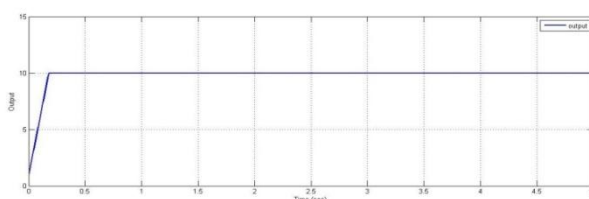


Fig.11 performance of anti wind up system (Time Vs Output)

The output of the load current in balanced condition are shown in the fig .10 .PID anti wind up system is proposed and designed in this is system ,when the speedup wind will exceeds critical speed the anti wind p system will limit wind speed.

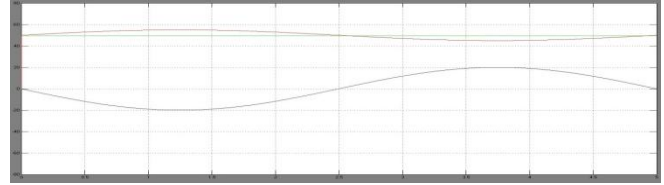


Fig.12 Input, output, and super capacitor powers (Time Vs MW)

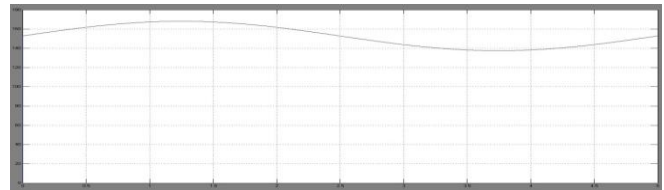


Fig.13 generator speed(Time Vs RPM)

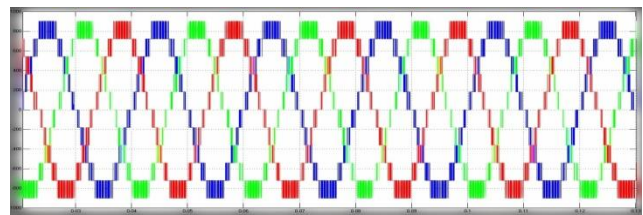


Fig .14 Inverter output current in an imbalanced condition(Time vs Voltage)

Fig 12 shows input and output powers and also draw super capacitors powers .Fig.13 shows the generator speed along with variation of the wind speed .the respective speed of generator in RPM.Fig.14 explains the inverter output voltages in imbalanced condition .

CONCLUSION

A capacitor-clamped three-level grid-side inverter-based super capacitor direct integration scheme has been proposed in this paper for mitigating short-term power fluctuations in wind power systems. In order to get the optimum use of super capacitors, they should be operated under variable voltage conditions. Increase in the blocking voltage is a concern with this variable voltage operation which can be solved with the use of high voltage switching devices such as SiC. The issue of thermal overrating of heat sink associated with the proposed super capacitor direct integration scheme needs further analysis. The major modulation challenge of the variable voltage operation is the uneven distribution of space vectors. The effects of this phenomenon are discussed in this paper followed by a proposition of an appropriate SVM method.

The proposed modulation method is capable of producing desired outputs even in the presence of unevenly distributed space vectors. A small vector selection-based controller is also proposed to control the super capacitor charging/discharging process with voltage equalization. Simulation and experimental results prove the efficacy of the proposed modulation method and charge/discharge controller.

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