ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 2, Issue 1, January 2014

Digital Beam Former Architecture for Sixteen Elements Planar Phased Array Radar

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Abstract- Beam forming is a signal processing technique used in antenna arrays for directional signal transmission or reception. Phased array radar is very important in modern radar development, and multiple digital beams forming technology is the most significant technology in phased array radar. Digital multiple beam forming on each antenna element about large phased array radar is impossible in processor based digital processing units, because it needs simultaneous processing many A/D channels.

This paper describes architecture for a digital beam former developed for 16 element phased array radar. The digital beam former architecture includes the complex operations such as down conversion which is done in parallel for the signal coming from each of the antenna elements and the filtering. A high performance FPGA is employed to perform these operations. An echo signal of 5 MHz riding on the IF signal of 60 MHz is down converted digitally to the baseband of the echo signal. The baseband echo signal is then multiplied by the complex weights and then summed to form the beam. The prototype architecture employs 16 bit 125 MS/s ADCs and a very high performance state of the art Xilinx FPGA device Vertex 6vlx240t to form the 112/4/6/9 beams simultaneously. The device used has large number of on chip resources for the parallel processing and the 200MHz clock generator. The complex weights are externally calculated using highly stable Q-R decomposition based recursive least squares algorithm and stored inside the FPGA.

Keywords-DBF, FPGA, QRD-RLS, DDC, CIC filter, ASIC, Nyquist Zone.

1.INTRODUCTION

As phased array technology has progressed, the use of solid state radar systems has become diversified [1]. A single array may now be used for a variety of purposes including communications, weather sensing, and aircraft tracking. Both the hardware specialization and dynamic reconfigurability offered by contemporary FPGAs offer unique opportunities to customize beamforming to specific application needs. FPGA hardware can be specialized to focus the radar beam in one or more directions and dynamic FPGA reconfiguration can be used to allow the phased array to support multiple sensing tasks.

As the required sensing task changes, a new beamforming design is swapped into the FPGA. Systems such as radar receiver [10][11] which are designed to receive spatially propagating signals often encounter the presence of interference signals. If the desired signal and interference occupy the same frequency band, then temporal filtering cannot be used to separate signal from interference. However, the desired and interfering signal usually originate from different spatial locations. This spatial separation can be exploited to separate signal from interference using spatial filter at the receiver When the spatial sampling is discrete, the hardware that performs spatial filtering is termed as beam former [3]

Digital beam forming [9] has many of the advantages a digital computational environment has over its analog counterpart. In most cases, less power is needed to perform the beam steering of the phased array antenna [10][11]. Another advantage is the reduction of variations associated with time, temperature, and other environmental changes found in analog devices.

Digital beam formers can accomplish minimization of side-lobe levels, interference cancelling and multiple beam operation without changing the physical architecture of the phased array antenna. Every mode of operation of the digital beam former is created and controlled by means of code written on a programmable device of the digital beam

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former, in this case a Xilinx FPGA[51[6l. As all the operations are performed digitally, the received RF analog signal at each antenna element is first converted to digital form using high speed multi- byte parallel ADCs.

The high speed samples from ADC are fed to digital down converter to get two down converted signals, a signal in-phase with the input and another in quadrature phase with the input. These I and Q components are then fed to complex multiplier where they are multiplied with the weights stored inside FPGA block RAMs. Finally the outputs of all the complex multipliers are summed to form a beam. A main lobe is produced together with nulls and side lobes.

The formation of multiple beams depends highly on the sampling rate of ADCs, processor computational capacity and the operating frequency of the processor. Thus the main components involved in implementation of digital beam forming are as follows.

- High speed parallel ADCs to convert incoming RF signal at each antenna element to the digital signal accurately•
- The digital down converters which brings down the high sample frequency from the ADCs to the baseband frequency, in order to enable to process the data at lower rates.
- Algorithm for computation of weights which are used to weigh the input signal to obtain the desired radiation pattern.
- High speed data communication path for receiving weights and sending beams for further processing and plotting.This paper addresses several issues involved in the design and implementation of a digital beam former architecture which is developed for 16 element planar phased array radar.

II. OPTIMUM WEIGHT CALCULATION

The application of QR decomposition to triangularize the input data matrix results in an alternative method for the implementation of the recursive least-squares (RLS).

The main advantages brought about by the recursive least-squares algorithm based on QR decomposition [4][[2] are its possible implementation in systolic arrays and its improved numerical behavior when quantization effects are taken into account. Weights w(n) corresponding to each antenna element at time t_n can be found out using RLS algorithm as follows.

$$R_{xx}(n)w(n)+p(n)=O \quad (1)$$

Here, Rxx is the (M-[)*(M-1) data covariance matrix X, where M is the number of sensors, and p(n) is the (M-l) element cross correlation vector.

The QR decomposition [4][12] of a matrix is the decomposition of the matrix into an orthogonal and a triangular matrix. This matrix decomposition can be used to solve linear systems of equations like the linear least squares problem.

The QR decomposition [4][[2] can be applied to the least squares problem given above as:

$$Q(n)X(n)=((R(n)):o) \quad (2)$$

Where, Q(n) and R(n) denote (M -[)*(M -1) orthogonal matrix and (M -1)*(M -1) upper triangular matrix respectively. Since Q(n) is an orthogonal matrix the residue vector e(n) can be evaluated as:

$$I\,e(n)i = I\,(R(n):O)w(n)+((u(n)):(v(n) \quad (3)$$

Where,

$$((u(n)):(v(n)))=Q(n)d(n) \quad (4)$$

The den) denotes the reference data of the systolic array. The RLS weight vector that minimizes Ile(n)11 can be computed by:

$$R(n)w(n)+u(n)=O \quad (5)$$

The advantages offered by QRD-RLS algorithm[4][12] over the conventional RLS algorithm are as follows:

- Directly deals with observed data matrix
- Achieves the requirements of computational efficiency
- Achieves robust numerical stability as there is no sample matrix inversion.

II. BACKGROUND

A. Digital Beamforming

The ability to transmit and receive RF energy in a specific direction plays a crucial role in all radar applications.Forming a beam and electronically scanning it over a range of space can be done using an array of antennas with input/outputs that can be phase shifted with respect to

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one another. On receive, *phased array* beamforming is performed by taking advantage of the time delay of a wavefron as it reaches different antenna locations in the array. If the wavefront arrives broadside to the array ($\theta = 0$), the wavefront will reach each element at the same time and produces a signal s(t). However, if the wavefront hits the array at an angle, the signal received at an element will be delayed relative to its neighbor by an amount proportional to the element spacing and the angle of incidence. This effect is illustrated on the left in Fig. 1. The signal at the m_{th} element will be $s_m(t) = s(t - mt_d)$ where $td = X/c_o = dsin(\theta)/c_o$ and c_o is the speed of light.

To maximize the signal received from a particular direction, a beamforming system imposes a compensating delay, mto, on the received signal at the m*th* element and then combines all M signals to form signal C as described by

$$C = \sum_{m=0}^{M-1} a_m s_m(t + mt_o) \qquad (1)$$

where a*m* is an amplitude weighting factor that is sometimes used. When the angle θ is such that t*d* = t*o*, then the delay compensated signals are aligned and they reinforce each other, maximizing C. Wavefronts coming from other angles will have different delays that are not equal to t*o* and the beamformer will not align them. Gain can be greatly reduced for those signals.

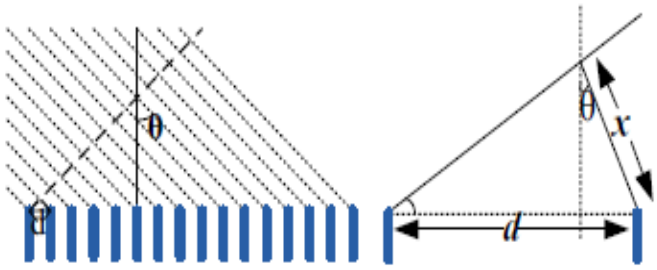

Figure 1. A linear array of antennas with a plane wave with angle of arrival θ. Antennas in the array are spaced at distance d

$$s_m(t) = Re\left[(I + jQ)e^{j\omega(t - mt_d)}\right] \qquad (2)$$

where I and Q are slow functions of time (several MHz) which carry the magnitude and phase information that the receiver is required to detect. When written in the complex signal form, the modified m*th* signal becomes,

$$a_m s_m(t + mt_o) = Re\left[(I + jQ)(a_m e^{j\omega mt_o})e^{j\omega(t - mt_d)}\right] \qquad (3)$$

where the second term on the right hand side is a complex weight which includes the amplitude weighting and delay found in (1). In (3) it can be seen that, when the incidence angle θ is such that t*d* = t*o*, then the m dependent terms in the exponent cancel and all element signals in (1) sum constructively.

In an analog beamformer, the weighting and summation operations occur at high frequency whereas a digital beamformer performs weighting and summing digitally at baseband frequencies. This paper is focused on digital beamforming, which is gaining in popularity for contemporary radar systems.

1) Beamforming Preprocessing*:*

Before digital beamforming operations can take place, each received antenna signal is subjected to a series of preprocessing steps including *downconversion*, *sampling*, *demodulation*, and *filtering*. The signal, s*m*(t), received by the m*th* antenna element is downconverted to an intermediate frequency (ωt $\rightarrow$ ωIF t) and filtered to remove spurious channels (such as the image channel). In our application, signals are downconverted from near 10 GHz to a 60 MHz intermediate frequency (IF). These signals have an information bandwidth of 12 MHz.

2) Digital Beamforming Operations:

Digital beamforming occurs when the delayed baseband sequences represented by (4) are weighted and summed so that:

$$I_m + jQ_m \equiv [I + jQ]e^{-j\omega mt_d} \qquad (4)$$

$$\sum_{m=0}^{M-1} (I_m + jQ_m)\, W_m = (I + jQ)\, AF(\theta) \qquad (5)$$

$$AF(\theta) = \sum_{m=0}^{M-1} e^{-j\omega mt_d} a_m e^{j\Psi_m} \qquad (6)$$

W*m* is the weighting factor introduced in (3), W*m* = a*m*cos(Ψm) + ja*m*sin(Ψm), and Ψm = mωto (see also, (3)). AF(θ) is called the *array factor*. The outputs of the beamformer are two sequences, the real and the imaginary parts of the right side of (5). I and Q are time dependent (functions of nt*s*) and contain the baseband information, but have no θ dependance. The array factor depends on θ, but is

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INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 2, Issue 1, January 2014

not time dependent. Although it is complex, its magnitude is the important part.

B. FPGA based Digital Beamforming Systems

Digital beamforming using FPGAs has become a popular technique for many military and commercial radar systems. Generally, these systems have the following characteristics:

1) Multiple boards of ADC and FPGA components are required to sample numerous analog channels and integrate partial beamforming results.

2) The beamforming hardware implemented in the FPGA is generally static throughout the operation of the radar system except for possible beamforming coefficient, W*m*, updates.

3) The cost associated with a multi-board beamforming system is often greater than $100,000. Several recent research projects have used FPGAs to perform beamforming. A multi-component system [2] uses five separate cards and samples up to 20 analog channels with individual ADCs. Five Virtex II devices are subsequently used to form up to four beams. A larger system.

[3] uses 32 separate ADC boards to sample radar signals at 100 MHz. Sampled data is then transmitted serially to a single Virtex II device via optical fibers. A single beam is formed within the FPGA.

C. Dynamic FPGA Reconfiguration

The flexibility of contemporary FPGAs extends beyond their ability to implement specialized logic. These SRAMbased devices can be reconfigured in the field, often while system operation progresses.

In the case of beamforming, the number of beams, the data rate of the sampled data, and the amount of FPGA power consumption may all be factors in determining the benefit of dynamic FPGA reconfiguration. Previous FPGAbased systems have shown the ability to significantly reduce power consumption by swapping in more power-efficient hardware when less FPGA processing is required. In contrast, in this paper, the ability to support multiple real-time applications is addressed.

III. REALIZATION OF DBF

The Block diagram shown in Fig. 3 explains the architectural features of the DBF for Four element Phased Array antenna [10][1 I].

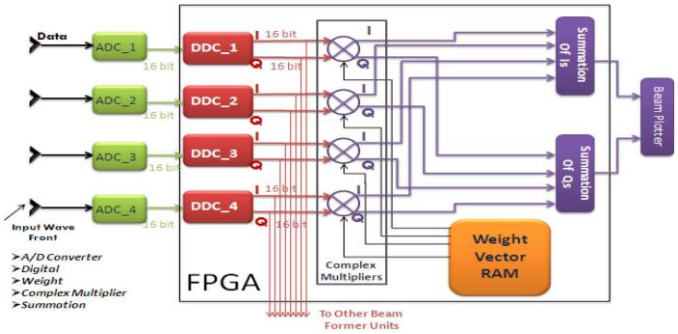

Fig. 1. Block diagram of a four element DBF for multiple digital beams.

This Architecture has been extended to [6] element array in this work and the same can be extended to any number of antenna arrays. The basic building blocks for this development are Digital down converters (DDC), complex adders and complex multipliers. The [F] signal, generally in the range of 50MHz to 60 MHz is converted into one word digital data using 8/ [6 bit, 125 MS/s high speed ADCs. The digital data is received at a sampling clock of 50 MHz and then processed as follows: 16 bit high speed ADC Data is passed through a digital Mixer consisting of a 50 MHz Numerically Controlled Oscillator (NCO), a multiplier (16x16 bit), suitable low pass decimation and compensating filters (C[C and CF[R filters) of bandwidth 5 MHz to filter the entire unwanted signal outside the band and a [0 rate decimator to bring down the sampling rate to 5 MS/s for further processing Finally the DDC output will be [n phase (I) and Quadrature (Q) signals. Fig. 2 gives the architectural details.

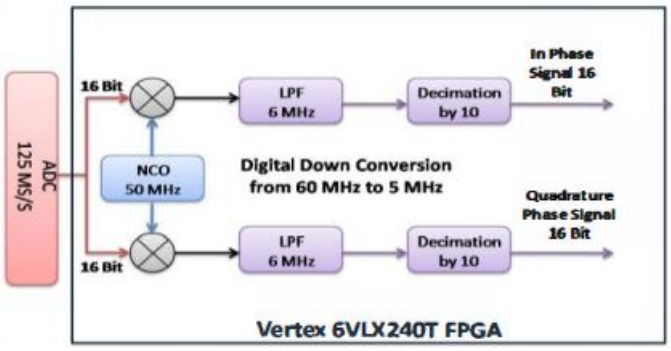

Fig.2. FPG A Based Digital Down Convertor

A straightforward implementation uses two multipliers, one each for the sine and the cosine as shown in Fig.3.

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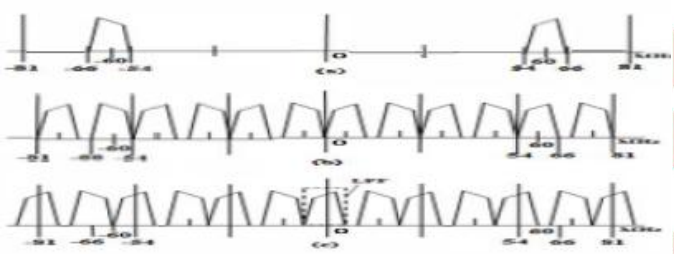

Fig.4. Nyquist Zones for fc = 60 MHz and fs = 50 MHz

The multipliers are 16 x 16 bit signed multipliers. The lower 16-bits, of the 32-bit output, are truncated and the 16 most significant bits are used for subsequent processing. The quantization error is within 0.1 % and is acceptable.

For realizing the 16 element array it is essential to have 16 different DOC modules in the complete architecture. Details are shown in the Fig 5. The complex multipliers and complex adders are implemented in hardware using VHDU141. To perform this complex multiplication in FPGA we need to perform equivalent floating point arithmetic operations in fixed point as the error is within limits and this is faster. The weights are calculated and stored in the memory of the FPGA. Depending upon the signal available from any direction within the range from _45° to +45°, suitable weights will be applied and the required number of beams will be calculated. During the formation of the beams it is assumed that direction of arrival is known apriori as the transmit beam is scheduled by the radar computer. With respect to the direction of arrival, multiple beams are fonned. The offset is fixed by the weights which are calculated and stored in the memory. With the developed architecture the weights are calculated for +1-10, +1- 20 and so on.

It is required to compute the complex multiplication for several numbers of weights which will decide where the beam needs to be fonned. For sixteen elements to form one beam we need to have sixteen weights and for N number of beams, N different sets of sixteen weights are required. We consider the weights are fixed and calculated offline.

The data flow architecture of the complex addition and complex multiplication are shown in Fig. 5 which is simulated using VHDU141 modeling and implemented on the prototype development hardware shown in Fig. 6. Summation of all the partial beams in the same digital domain, gives the full beam B(t), given by equation 6 for an N-element Array .

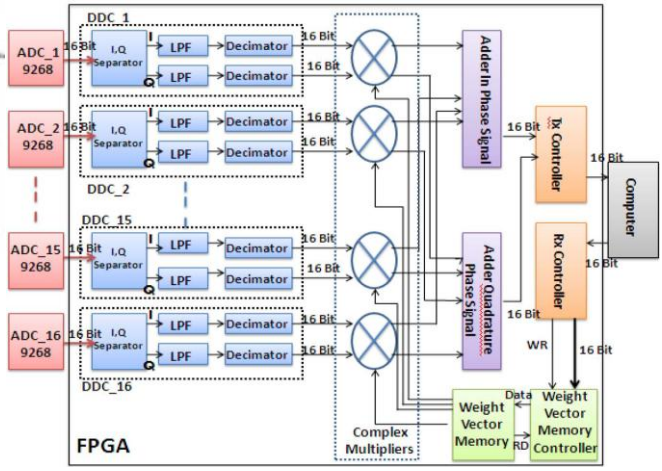

Fig.5. Digital Beam Former Architecture for 16 element array.

Where, N is Number of T IR Elements, W k is Complex Weight of Klh Element, S (t) is Received Signal

$$B(t)=_{k=0}\sum^{N} S_k(t)*W_k \quad (6)$$

The Development Hardware used to implement digital beam former architecture for 1/2/4 beams is shown in Fig.7 below:

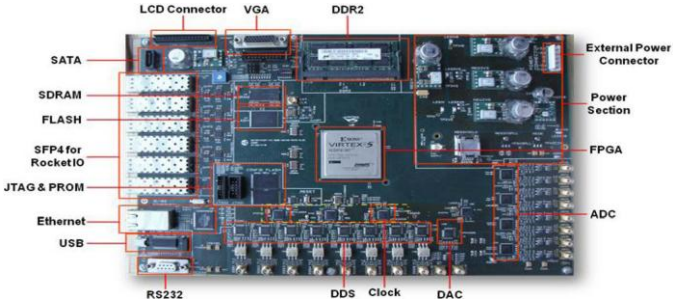

Fig.6. Prototype Hardware (Virtex 5) for 16 element array Digital Beam Former.

This modular design approach can also be used for ASIC design in the later stage of the development. The main features of the prototype developed are:

- FPGA - Virtex 5 FX130T[51
- Clock Domains:

Onboard Clock Oscillators : 32 MHz
Clock distribution for ADC, DAC and DDS using CDCE62005 (Texas Instruments) with external clock input on SMA.

- Memory

2 GB DDR2 - SDRAM using MT16HTF25664H- 667B
256Mb Flash Memory - JS28F256P30T95 from Numonyx
128 Mb SDRAM Memories - MT48LC4M32B2 from Micron

- Rocket 10 interface @ 3.125 Gb/s

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Six SFP connectors are provided for SFP modules

- Analog Input

Four, Two channel using, 16 bit, 125 MSPS ADC: AD9268 from Analog Devices

- Analog Output

One, Two channels using, 14 bit, 125MSPS DAC: DAC2904 from Texas Instrument

Eight, single channel, DDS : AD9954 from Analog Devices

- External Interfaces: Ethernet, USB 2.0 High Speed, Two RS-232 channel using MAX3223 on DB9, L VDS Interface.

The Development Hardware used to implement digital beam former architecture for 6/9 beams is shown in Fig.7 below:

- FPGA- Virtex - 6 LX240T - I FF I156C [6].
- Clock

Onboard Oscillators: 32 MHz, 156.25 MHz clock oscillator for SFP

- Memory:

1GB DDR2 SDRAM using MT8HTF I2864H-667B. 256Mb flash Memory - JS28F256P30T95 from Numonyx.

- Rocket 10 interface @ 3.125 Gb/s: Four SFP connectors are provided for SFP modules. PCI Express : 8x lane @ 2.5 Gb/s
- USB 2.0 High Speed: Using Cypress chip CY7C680 13A.

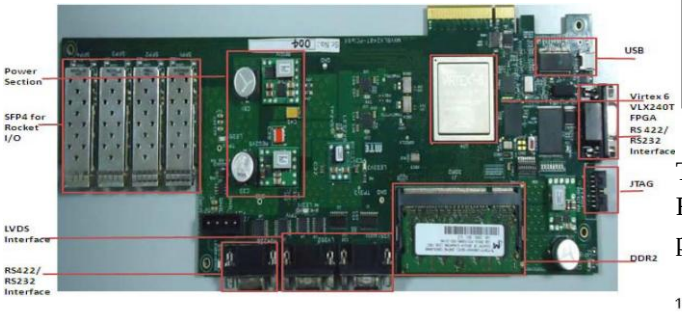

Fig.7. Prototype Hardware (Virtex 6) for 16 element array Digital Beam

The tools used for the implementation of 16 element antenna array Digital Beam Former are given below.

- Matlab for modeling purpose.
- ISE for implementation.
- Symplify Pro for synthesis.
- ISE Simulator for functional simulation.

IV. RESULTS

The implementation for forming four beams is done on Vertex 5 series FPGA [5] having high speed ADC 9268 on board. The resource utilization for this implementation is given in table 1.

The implementation of DBF for more than 4 beams is done on Vertex 6 series FPGA [6] due to the requirement of more resources for parallel processing. On this board the input is given from DDS inside the FPGA which corresponds to 60 MHz output of the ADC. The resource utilization for this implementation is given in table 2.

TABLE 1. Resource utilization for implementation of DBF for 4 beams on Vertex 5 FXI30T FPG A

Sr. No	Slice Logic Utilization	Used	Available	Utilization
1	Number of Slice LUTs	43,803	81,920	53%
2	Number of Block RAM/FIFO	38	298	12%
3	Number of BUFG	4	32	12%
4	Number of DSP48E	298	320	93%
5	Number of PLL_ADVs	1	6	16%

T ABLE II. Resource utilization for implementation of DBF for 9 beams on Vertex 6 LX240T FPG A

Sr. No	Slice Logic Utilization	Used	Available	Utilization
1	Number of Slice LUTs	86,983	150,720	57%
2	Number of Block RAM/FIFO	50	416	12%
3	Number of BUFG	6	32	18%
4	Number of DSP48E1	634	768	82%
5	Number of PLL_ADVs	1	12	8%

The beams are plotted in the Matlab. Weights are taken from FPGA to Matlab, multiplied with scanning vector and then plotted.

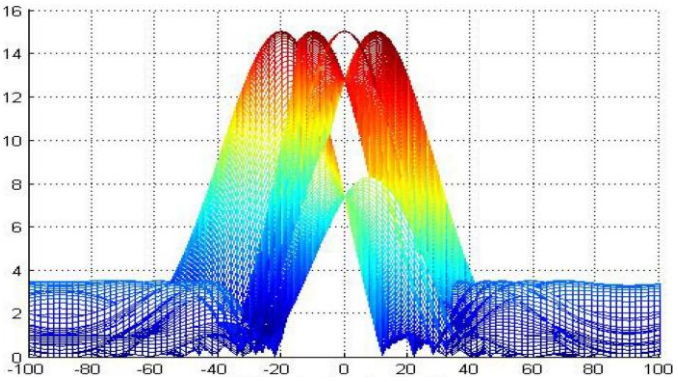

Fig.IO. Four beams plotted in Matlab using the weight vectors stored inside FPGA

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V. ADVANTAGES

1.Reducing of the area consumption in FPGA hence results in low cost and low power.
2.Provides all time output hence no need of reconfiguration or reprogrammability technique.
3. Since digital logic, the beam can be steered by changing the weight factors.

VI. CONCLUSION

We have developed a 16-element phased array multiple DBF system. The weights are calculated using the highly efficient QRD-RLS [4][12] algorithm. The Virtex-V FPGA is used for the spatial digital processing for 4 beams and VirtexVI FPGA is used for 6/9 beams, and it has enabled a remarkable reduction in the area utilization compared to the discrete and analog versions. This pipelined architecture generates multiple beams up to maximum of 9 beams simultaneously from a given array matrix of 16 elements. Conventional methods of implementation of beam forming make the system cumbersome and sensitive to temperature and other unavoidable environmental conditions. FPGA[5][6] based implementation finds huge applications in modern radars as this implementation makes the system immune to the limitations that the analog methods face. At the same time, the proposed beam-forming system enjoys advantages of a reconfigurable design and low cost. The next step for enhancing the DBF system is including online weight calculation algorithm such as QRD-RLS [2][4][12], inside the FPGA, so as to enable radar to track the changes in continuously varying environment. Thus making DBF system robust and efficient.

ACKNOWLEDGEMENT

We are thankful to Mr. Rakesh Mehta, Director and his team from Mis BMIT, Pune for helping us to realize the proposed system hardware. Thanks are also due to Mr. Haseen Basha, Scientist, LRDE for helping us in the implementation of the DDC as part of the DBF.

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