



Simulation Modelling on Harmonic Reduction Using Cascaded Multilevel Inverter fed Induction Drive

Dr.T.Govindaraj¹, P.Vijayakumar²

Prof and Head- Department of EEE, Muthayammal Engineering College, Rasipuram, Tamil Nadu, India¹

Research Scholar-M.E Power Electronics and Drives, Muthayammal Engineering College, Rasipuram, Tamil Nadu, India²

Abstract: In this project, a multilevel inverter was designed and implemented to operate a stand-alone solar photovoltaic system. The proposed system uses selective harmonics elimination pulse-width modulation (PWM) in the multilevel inverter to convert DC voltage from battery storage to supply AC loads. In the PWM method, the effectiveness of eliminating low-order harmonics in the inverter output voltage is studied and compared to that of the sinusoidal PWM method. This work also uses SHEPWM to predict the optimum modulation index and switching angles required for a nine-level cascaded H-bridge inverter with improved inverter output voltage. The proposed predictive method is more convincing than other techniques in providing all possible solutions with any random initial guess and for any number of levels of a multilevel inverter. The simulation results prove that the lower-order harmonics are eliminated using the optimum modulation index and switching angles. An experimental system was implemented to demonstrate the effectiveness of the proposed system.

Keywords: SHEPWM, Redundant states, Self-balancing, Harmonic Reduction, Cascaded MultiLevel Inverter

1. INTRODUCTION

In recent years, environmental concerns the depletion of fossil fuel reserves have spurred significant interest in renewable energy sources. Interconnecting these intermittent sources to the utility grid on a large scale it affect the voltage/frequency control of the grid and lead to severe power quality issue. Multilevel inverter has been attracting extensive attention from as well as industry in the recent decade [1]. They have emerged as the solution too many problems related to the traditional two-level inverter. The principal advantage is to generate a good waveform quality reducing the voltage stresses on power semiconductor devices. So, they are very useful in high power ac applications. Several multilevel-PWM methods are developed for the two-level inverter and expanded to the multiple levels. The most popular are the multilevel carrier-based PWM

derivatives. However, these techniques offer good performances using high switching frequency [2],[9]-[21]. The SHEPWM-based method can theoretically provide various performance advantages over all the PWM methods. These advantages include, produced the desired fundamental sinusoidal voltage while at the same time

certain order harmonics are eliminated [3]. Otherwise, the use of this kind of inverter poses the dc-link capacitor unbalance problem. Two main approaches have been proposed. 1) The use of additional passive and/or active components. 2) The manipulation of the redundant switching states. The first solution causes an increase of system cost and additional power losses. For the second one, it is generally used in the space vector PWM. In fact, this paper shows that the redundant states can be associated to the selective harmonic elimination PWM in order to improve more and more the performance system in term of quality signal and power losses. In order to reduce energy loss in transmission lines and increase the overall battery capacity, the battery bank is series connected for a high-voltage dc power supply[2]-[8].

2. SELECTIVE HARMONIC ELIMINATION

This is also termed as the optimized PWM technique. By reversing the phase voltages a few times during each half cycle, it is possible to eliminate lower order harmonics selectively. However, the higher order harmonics may increase in magnitudes, but the current harmonics are not significantly affected due to low pass filter characteristics of the AC system. The voltage reversals are affected at chosen instants such that the notches (caused by the voltage reversals) are placed symmetrically about the centre line of each half cycle. If there are 'p' switching (voltage reversals)

in a quarter cycle, the rms value of the nth harmonic voltage is given by,

$$E_n = \pm \frac{0.45}{n} V_m [2(\cos n \alpha_1 - \cos n \alpha_2 + \cos n \alpha_3 \dots) - 1] \quad (1)$$

Where $\alpha_1, \alpha_2, \dots, \alpha_n$ are switching angles within each quarter cycle. There are p degrees of freedom and are used to cancel (p-1) harmonic components in the voltage and control the fundamental voltage. For example, if there are 3 switching at α_1, α_2 and α_3 , we can eliminate the fifth and seventh harmonics in addition to

control the fundamental voltage. We get 3 transcendental equations is given by,

$$m = 2[\cos \alpha_1 - \cos \alpha_2 + \cos \alpha_3] - 1 \quad (2)$$

$$0 = 2[\cos 5 \alpha_1 - \cos 5 \alpha_2 + \cos 5 \alpha_3] - 1 \quad (3)$$

$$0 = 2[\cos 7 \alpha_1 - \cos 7 \alpha_2 + \cos 7 \alpha_3] - 1 \quad (4)$$

Note that although the phase voltage contains triple harmonics, the line to line voltages are free from them [7]-[8].

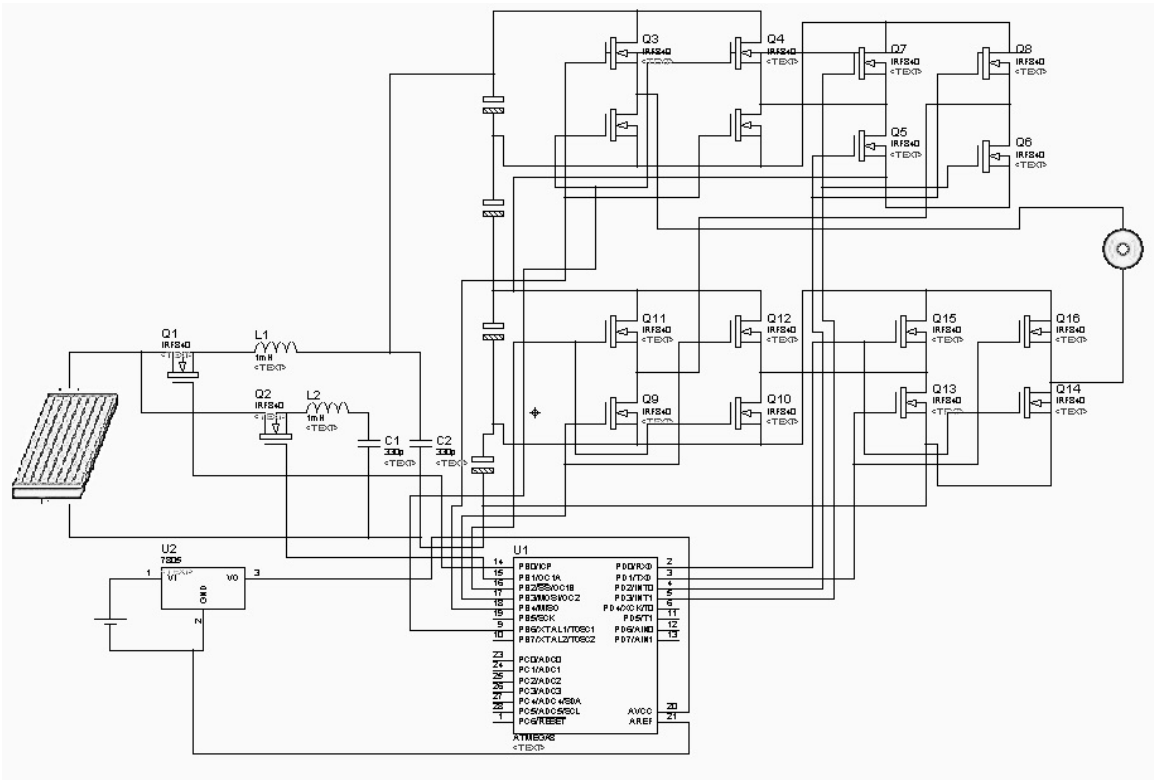


Fig 3.1 Circuit Diagram

3. CIRCUIT DIAGRAM

3(A) Operation of Circuit Diagram

In order to keep the four voltages equal, we will make use of the switch states of the 9-level inverter. Three groups are distinguished from 125 switch states. The first one is formed by 24 vectors which do not connect any of the phases to the common capacitors potential and so the capacitor voltages remains unaffected. The second group has 36 vectors with multiple switch states. The last one is the vector zero with five different switch states. They have

group will be used to ensure the capacitor voltages balance. Different switch states force load current to flow through different paths. Thus the direction of current through the DC-link capacitors is different and variation of capacitor voltages is minimizing the difference between the voltages of the four capacitors by selecting the suitable redundancy among the different. We express the capacitor currents by the two ac load current i_a and i_b .

According to their sign, we can know the effect of each state on the capacitor behavior (charge or discharge). voltage vectors of group 2. The switch state selected has to unload the most loaded capacitor voltage and load the unloaded one. Therefore, capacitor voltage derivations have to be considered. Substitute the modulation 1 1 4 by the first redundancy (0 0 3) which allows charging C_1 and

discharging C_d . In the contrariwise, we let the initial state. The same operation is done using the PWM signal given by the SHE technique at the end; we obtain another leg voltage waveform which provides the same modulation voltage and the same harmonics spectrum. The proposed capacitor balancing method has been assessed by simulation.

4. SIMULATION CIRCUIT DIAGRAM

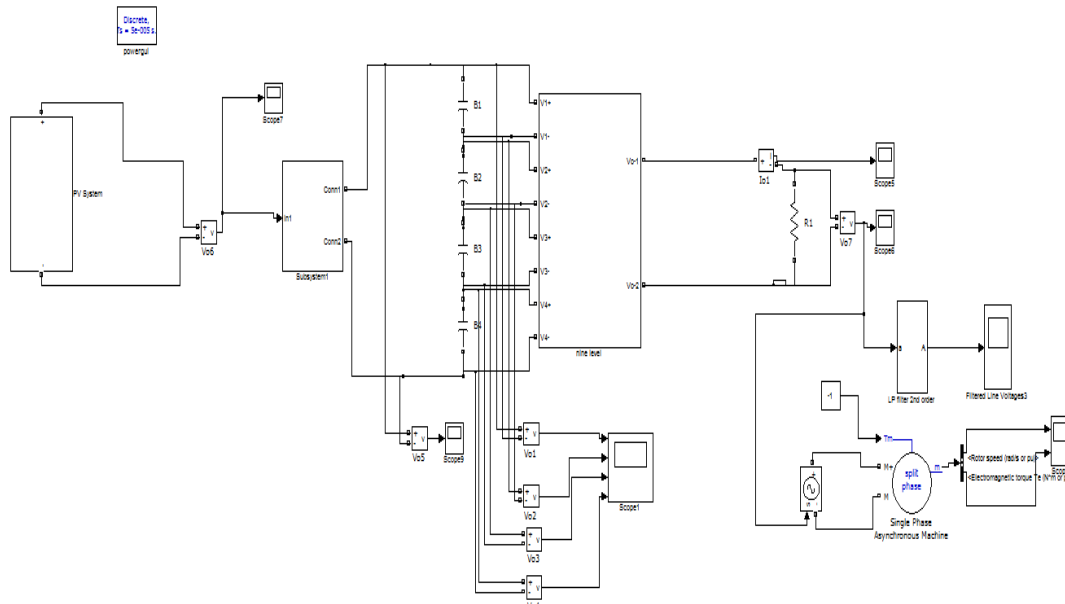


Fig 2 Simulation circuit for 9-level Cascaded Inverter

4 (A) Simulation Results

The proposed nine-level inverter circuit has been tested on a 230V, 50Hz, induction motor drive with V/f control scheme at a switching frequency of 1 kHz. This simulation diagram is drawn in MATLAB Software package. In this diagram, MOSFET Switches are connected in structure of cascaded with H-bridge. SHEPWM technique is used in this project for controlling the inverter by giving gate pulse to MOSFET Switches. The inverter dc-link voltage is set to 230 V. The hysteresis limit for the capacitor is set at 5% of the respective capacitor voltage. The capacitors are sized suitably so that the voltage of the capacitors would not cross the hysteresis limit in two switching cycles at full load current. Simulation circuit for nine-level in switching angles is calculated by give the firing pulses to the nine level inverter, the staircase voltage waveform is obtained. The FFT analysis is done in both the cases. The THD calculated in case of resistive load is 14.49% while in case of RL load is further reduced to 3.08%. The calculation revealed that 3rd, 5th and 7th harmonics is significantly reduced up to four decimal places and thus overall THD% is reduced. A full-bridge inverter or so-called H-bridge cell is introduced. Basically, an H bridge cell can generate up to

three output voltage levels. The appropriate gate control signal and blinking time are presented. Multilevel inverter using cascaded-inverter with SDCSs is introduced in both single-phase and three-phase structure. The output voltage is

the sum of the output voltage of each H-bridge cell. In three-phase system, the voltage THD can be improved in line voltage. Finally, the reason to use SDCSs is explained the concept of the optimized harmonic stepped-waveform technique will be presented.

4.1 OUTPUT VOLTAGE WAVEFORM

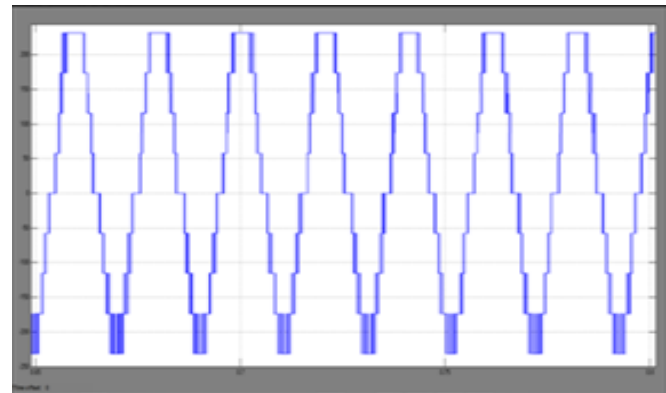


Fig.4.1 Output Voltage Waveform

4.2 OUTPUT CURRENT WAVEFORM

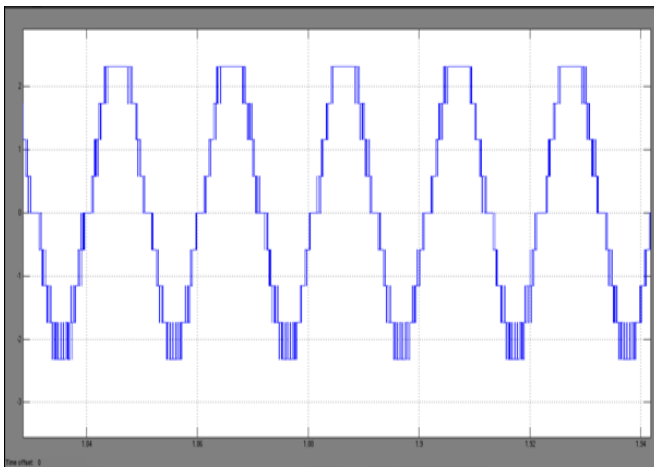


Fig.4.2. Output Current Waveform

4.3 FILTERED OUTPUT VOLTAGE

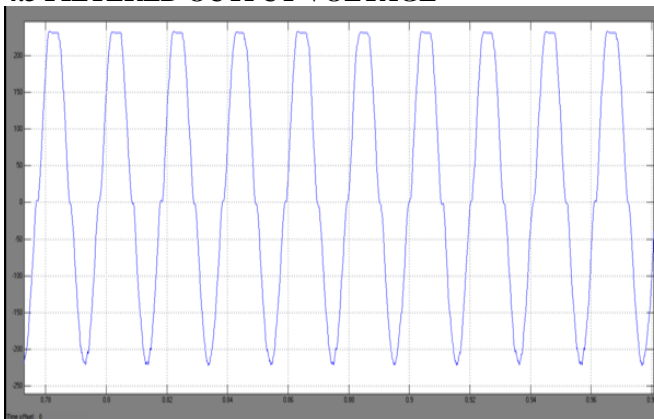


Fig.4.3. Filtered Output Voltage Waveform

4.4 THD ANALYSIS OF OUTPUT VOLTAGE

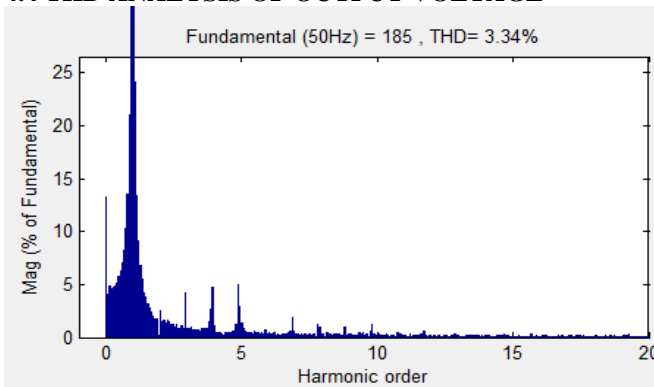


Fig.4.4. THD Analysis of Output Voltage

In this project, modulation index is 0.8 is used in pulse generator. The gate pulses are given to inverter through the subsystem. From subsystem the pulses are given to Goto and then Goto are linked with from blocks then pulses given to switches. Then output current and output voltage is

determined from the simulation results. The single phase induction motor is connected in this circuit. The THD analysis of output current and output voltage are determined by the simulation. The main advantages of this project are harmonics reduction. The THD percentage of the output voltage is 3.34%. When compare to other topology it has better harmonic reduction properties

5. CONCLUSION

Both optimization of switching angles of nine-level output waveform using SHEPWM and DC-link voltages balance are investigated in this study. The programmed PWM allows eliminating harmonics row 5, 7 and 9th orders with a good control of the fundamental voltage. In order to keep as well as possible the four capacitor voltages equal, we have made use the 61 switch states of the nine-level inverter. Its matrix representation simplify the redundant states analyse. The obtained results show the DC-link balancing while maintaining the SHEPWM performances.

6. REFERENCES

- [1] Chung-Ming Young, Neng-Yi Chu, Neng-Yi Chu, Liang-Rui Chen, Yu-Chih Hsiao, & Chia-Zer Li, "A Single phase multilevel inverter with Battery Balancing", IEEE Transactions on Industrial Electronics, Vol 60, No 5 May 2013.
- [2] B. Y. Chen and Y. S. Lai, "New digital-controlled technique for battery charger with constant current and voltage control without current feedback", IEEE Transactions on Industrial Electronics, Vol. 59, no. 3, pp. 1545–1553, Mar. 2012.
- [3] Pablo Lezana, Jose Rodriguez, and Diego A. Oyarzun, "Cascaded Multilevel Inverter With Regeneration Capability and Reduced Number of Switches", IEEE Transactions on Industrial Electronics, Vol. 55, NO. 3, Mar. 2008.
- [4] Leon M. Tolbert, Burak Ozpineci, and John N. Chiasson, "A Five-Level Three-Phase Hybrid Cascade Multilevel Inverter Using a Single DC Source for a PM Synchronous Motor Drive", IEEE Applied Power Electronics Conference, APEC 2007.
- [5] R.Narmatha and T.Govindaraj, "Inverter Dead-Time Elimination for Reducing Harmonic Distortion and Improving Power Quality", International Journal of Asian Scientific Research, Vol.3, April 2013.
- [6] Dr.T.Govindaraj, and T.Srinivasan, "An Hybrid Five-Level Inverter Topology with Single-DC Supply fed Special Electric Drive," International Journal of Advanced and Innovative Research ISSN: 2278-7844, Dec-2012, pp 542-548
- [7] K.R.Padiyar, , "HVDC Power Transmission Systems", New Age International (P) Ltd., New Delhi, 2002.
- [8] Rashid M.H., "Power Electronics Circuits, Devices and Applications ", Prentice Hall India, Third Edition, New Delhi, 2004.
- [9] Dr.T.Govindaraj, and V.Purushothaman, "Simulation Modeling of Inverter Controlled BLDC Drive Using Four Switch," International Journal of Advanced and Innovative Research. ISSN: 2278-7844, Dec- 2012, pp 554-559.
- [10] Govindaraj Thangavel, Debashis Chatterjee, and Ashoke K. Ganguli, "Design, Development and Control of an Axial Flux Permanent Magnet Linear Oscillating Motor using FE Magnetic Analysis Simulation Models," Int. Journal of Electrical and Electronics Engineering, Oradea, Romania, October 2010
- [11] Govindaraj Thangavel, Debashis Chatterjee, and Ashoke K. Ganguli, "FEA Simulation Models based Development and Control of An Axial Flux PMLM," International Journal of Modelling and Simulation of Systems, Vol.1, Iss.1, pp.74-80, 2010
- [12] Dr.T.Govindaraj, and A.Kanimozhi, " Instantaneous Torque control of Small Inductance Brushless DC Drive," International Journal Of Advanced and Innovative Research. ISSN: 2278-7844, Dec-2012, pp 468- 474.



- [13] Dr.T.Govindaraj, and T.Keerthana,“ DFC And DTC Of Special Electric Drive Using PI And FLC, ” International Journal Of Advanced and Innovative Research.ISSN: 2278-7844, Dec-2012 ,pp 475-481.
- [14]Dr.T.Govindaraj, and T.Sathesh kumar, “New Efficient Bridgeless Cuk Converter Fed PMDC Drive For PFC Applications,” International Journal Of Advanced and Innovative Research, Dec- 2012, pp 518-523
- [15]Dr.T.Govindaraj, and B.Gokulakrishnan, “Simulation of PWM based AC/DC Converter control to improve Power Quality,” International Journal of Advanced and Innovative Research.ISSN: 2278-7844, Dec-2012, pp 524-533.
- [16] Dr.T.Govindaraj, and M.Jagadeesh, “Resonant Converter Fed PMDC Drive Using Soft Switching Techniques,” International Journal of Advanced and Innovative Research ISSN: 2278-7844, Dec-2012, pp 535-541.
- [17] T.Govindaraj, Rasila R,“Development of Fuzzy Logic Controller for DC – DC Buck Converters”, International Journal of Engineering Techsci Vol 2(2), 192-198, 2010
- [18]Govindaraj Thangavel, Debashis Chatterjee, and Ashoke K. Ganguli,“ Design, Development and Finite Element Magnetic Analysis of an Axial Flux PMLOM,” International Journal of Engineering and Technology,Vol.2 (2), 169-175 , 2010
- [19]Govindaraj Thangavel, Ashoke K. Ganguli and Debashis Chatterjee,“Dynamic modeling of direct drive axial flux PMLOM using FEM analysis” International journal of Elixir Electrical Engineering Vol.45 pp 8018- 8022, April 2012
- [20] G. Thangavel and A. K. Ganguli,“Dynamic Modeling of Directive Drive Axial Flux PM Linear Oscillatory Machine Prototype Using FE Magnetic Analysis”, Iranian Journal of Electrical and Computer Engineering, Vol. 10, No. 2, Summer-Fall 2011
- [21] Govindaraj Thangavel, Debashis Chatterjee, and Ashoke K. Ganguli,“FEA based Axial Flux permanent Magnet Linear Oscillating Motor,” International Journal THE ANNALS OF "DUNAREA DE JOS" UNIVERSITY OF GALATI F ASCICLE III, ELECTROTECHNICS, ELECTRONICS, AUTOMATIC CONTROL, INFORMATICS , July 2010.

BIOGRAPHY

Dr.Govindaraj Thangavel born in Tiruppur , India , in 1964. He received the B.E. degree from Coimbatore Institute of Technology, M.E. degree from PSG College of Technology and Ph.D. from Jadavpur University, Kolkatta, India in 1987, 1993 and 2010 respectively. His Biography is included in Who's Who in Science and Engineering 2011-2012 (11th Edition). Scientific Award of Excellence 2011 from American Biographical Institute (ABI). Outstanding Scientist of The 21st century by International Biographical centre of Cambridge, England 2011.



Since July 2009 he has been Professor and Head of the Department of Electrical and Electronics Engineering, Muthayammal Engineering College affiliated to Anna University, Chennai, India. His Current research interests includes Permanent magnet machines, Axial flux Linear oscillating Motor, Advanced Embedded power electronics controllers,finite element analysis of special electrical machines,Power system Engineering and Intelligent controllers.He is a Fellow of Institution of Engineers

India(FIE) and Chartered Engineer (India).Senior Member of International Association of Computer Science and Information. Technology (IACSIT). Member of International Association of Engineers(IAENG), Life Member of Indian Society for Technical Education(MISTE). Ph.D. Recognized Research Supervisor for Anna University and Satyabama University Chennai Editorial Board Member for journals like International Journal of Computer and Electrical Engineering,International Journal of Engineering and Technology,International Journal of Engineering and Advanced Technology (IJEAT).International Journal Peer Reviewer for Taylor &Francis International Journal “Electrical Power Components & System”United Kingdom,Journal of Electrical and Electronics Engineering Research,Journal of Engineering and Technology Research (JETR),International Journal of the Physical Sciences,Association for the Advancement of Modelling and Simulation Techniques in Enterprises,International Journal of Engineering & Computer Science (IJECS),Scientific Research and Essays,Journal of Engineering and Computer Innovation,E3 Journal of Energy Oil and Gas Research,World Academy of Science, Engineering and Technology,Journal of Electrical and Control Engineering (JECE),Applied Computational Electromagnetics Society etc.. He has published 132 research papers in International/National Conferences and Journals. Organized 40 National / International Conferences/Seminars/Workshops. Received Best paper award for ICEESPEEE 09 conference paper. Coordinator for AICTE Sponsored SDP on Soft Computing Techniques In Advanced Special Electric Drives, 2011. Coordinator for AICTE Sponsored National Seminar on Computational Intelligence Techniques in Green Energy, 2011.Chief Coordinator and Investigator for AICTE sponsored MODROBS - Modernization of Electrical Machines Laboratory. Coordinator for AICTE Sponsored International Seminar on “Power Quality Issues in Renewable Energy Sources and Hybrid Generating System”, July 2013.



P.Vijayakumar born in Erode, India, 1991. He received the B.E degree from Sengunthar Engineering college, Tiruchengode, 2012. Now he pursuing M.E degree in Muthayammal Engineering College, Rasipuram, India. His area of intrest in power Electronics,Electric drives and control.