ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 2, Issue 2, February 2014

An Efficient Bridgeless PFC Cuk Converter Based PMBLDCM Drive

Jomy Joy[1], Amal M.R[2], Rakesh R[3], Kannan S.A[4], Anna Raina[5]

M Tech Scholar, Power Electronics, Toc H institute Of Science And Technology, Ernakulam, Kerala, India [1]
M Tech Scholar, Power Electronics, Toc H institute Of Science And Technology, Ernakulam, Kerala, India[2]
M Tech Scholar, Power Electronics, Toc H institute Of Science And Technology, Ernakulam, Kerala, India[3]
M Tech Scholar, Power Electronics, Toc H institute Of Science And Technology, Ernakulam, Kerala, India[4]
Assistant Professor, Department of EEE, Toc H institute Of Science And Technology, Ernakulam, Kerala, India[5]

Abstract: A new bridgeless Cuk PFC converter driving a permanent magnet brushless DC motor drive is proposed here. In the case of a conventional BLDCM drive system there will be a rectifier and a PFC converter connected to the drive through a voltage source inverter. In this project it is replaced by a bridgeless PFC Cuk converter and the voltage source inverter connected to the PMBLDCMD. This improves the efficiency of the drive as well as maintains a unity power factor. This is because of the bridgeless topology introduced which does not have an input diode bridge rectifier. That is there will be less number of semiconductor switches in the current flowing path. The bridgeless Cuk converter is designed to work in discontinuous conduction mode. The proposed PMBLDM drive is designed with necessary controls and modeled in MATLAB Simulink and simulated results are presented. Also a comparison is made between proposed drive system and the conventional Cuk rectifier fed PMBLDCM drive.

Keywords: Cuk converter, Power factor correction (PFC), Bridgeless Cuk converter, low conduction losses, total harmonic distortion, permanent magnet brushless DC motor (PMBLDCM).

I. INTRODUCTION

The applications if PMBLDC motors are increasing in the day to day life because of its features like low maintenance, high efficiency, and wide speed range. More over it is rugged due to the permanent magnets on the rotor. The commutation in a PMBLDCM is done by a three phase voltage source inverter. The PMBLDCM can be used in various applications like air conditioning system, electric traction etc. In all these applications the drive system has long life, low running cost and reduced electrical and mechanical running stresses. But the condition is that the quality of the power supply should meet specific standards like IEC 61000-3-2.

A PMBLDCM has developed torque directly proportional to phase current and its back EMF, which is proportional to the speed**.** That is, it has a constant current in its stator windings with variable voltage across its terminals maintains constant torque in a PMBLDCM under variable speed operation [1]. Speed control scheme used is a normal PWM control. However, the control of VSI is done by electronic commutation based on the rotor position signals of the PMBLDC motor.

In conventional cases a PMBLDCM drive is fed from a single-phase ac supply via a diode bridge rectifier (DBR) followed by a capacitor at dc link. The capacitor draws current in short pulses. This will generate harmonics and yield poor PF, resulting in poor power quality. Therefore various PFC converter topologies are available in order to meet the required IEC 61000-3-2 standard.

Most of the PMBLDC drive from the supply via diode bridge rectifier and a capacitor. But the capacitor draws pulsated currents which results in harmonics due to an uncontrolled charging of the dc link capacitor. So PFC converters are implemented in front of the dc link capacitor in order to supply a constant DC current. Therefore, a PF correction (PFC) converter among various available converter topologies [3] is applicable for a PMBLDCMD. Among these topologies most of them use boost topology at them front end. But the switching losses are high due to the presence o f the diode bridge. This affects the efficiency of the whole drive system.

Several topologies are proposed in order to maximize the efficiency of power supply. Bridgeless topologies are one such converter which can reduce the switching losses by reducing the number of power semiconductor switches in the current conduction path [4] [5]. By using this bridgeless topology the input diode bridge is avoided and therefore conduction losses are reduced which yield a better efficient system. Mostly used converter topology is bridgeless boost converter. But it is applicable only for boost operation and moreover it has high start up inrush current and lack of galvanic isolation [4]. The proposed topology in [6] introduces a buck bridgeless converter but has the disadvantages like low output voltage, high output voltage ripple. The topology proposed in [7] a SEPIC converter has relatively high output ripple due to the discontinuous output current. So if these converters are used in a drive system disadvantages of those converters will decrease the efficiency of the whole drive system.

The cuk topology based converter offer various advantages ahead of the above topologies, such as such as easy implementation of transformer isolation, natural protection against heavy inrush current occurring at start-up or overload current, lower input current ripple, and less electromagnetic interference (EMI) associated with the discontinuous conduction mode (DCM) topology. The DCM is preferred over other modes for having some added advantages like natural near-unity power factor, the power switches are turned ON at zero current, and the output diodes are turned OFF at zero current[8] [9].

II. BRIDGELESS CUK CONVERTER

The bridgeless Cuk converter proposed in [10] yields the perfect result so that the drive system will be efficient as well as power factor is improved to unity. The proposed converter in Fig (1) acts as an AC-DC converter without an input diode bridge; so named as a bridgeless topology.

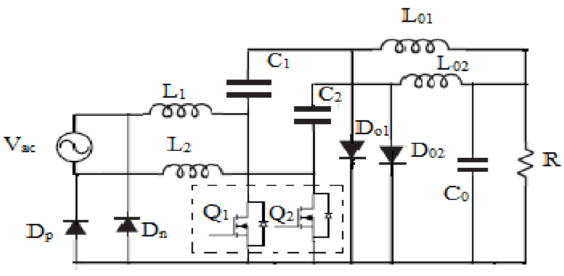

Fig 1: Bridgeless Cuk Converter [10]

The bridgeless Cuk converter has the advantage over the conventional cuk converter in the case of switching losses. Two DC–DC Cuk converters are connected as in Fig 1 to form the bridgeless topology. One of the Cuk DC-DC converters will operate for each half-line period (*T*/2) of the input voltage. According to Fig 1 there are one or two semiconductor(s) in the current conduction path. Therefore the current conduction losses in the active and passive switches are further reduced and the circuit efficiency is improved compared to the conventional Cuk converter. Common mode noise problem due to the pulsating output voltage with respect to the ground is a major drawback of almost all converters. So in order for balancing the circuit there by prevent the common mode noise problem, here output voltage is always connected to the input ac line through the slow-recovery diodes D_p and D_n. Thus, the proposed topology does not suffer from the high common-mode EMI noise emission problem.

As in the bridgeless converter shown in Fig (1) there are two power semiconductor switches, Q_1, Q_2 along with two recovery diodes D_p,. The switches can be driven by the same control with the condition that Q_1 will be ON at positive cycle of the input voltage and Q_2 vice versa. This can reduce the control circuitry complexity

Assume that the converter is operating at a steady state in addition to the following assumptions: pure sinusoidal input voltage, ideal lossless components. The output filter capacitor is large enough such that the voltage across it is constant. During the positive half cycle of the input AC, the first dc–dc Cuk circuit, L_1–Q_1–C_1–L_{o1}–D_{o1}, will be active through the positive diode D_p. This connects the input ac source to the output. During the negative half-line cycle, the second dc–dc Cuk converter circuit, L_2–Q_2 -C_2–L_{o2}–D_{o2}, is active through negative diode *Dn*, which connects the input ac source to the output.

The operation of the bridgeless rectifier is made in discontinues node by suitable design of the active and passive components like inductors, capacitors. By operating the rectifier in DCM, several advantages can be achieved. These advantages include natural near-unity power factor, the power switches are turned ON at zero current so less turn ON losses, and the output diodes (D_{o1} and D_{o2}) are turned OFF at zero current so turn OFF losses are reduced. The bridgeless topology has an additional inductor as compared with conventional topology which is a disadvantage but the topology will have good thermal performance.

III.CONVERTER DESIGN

The design of the converter is made as below with certain mathematical assumptions. The DCM operation is obtained with the following condition:

$$K_e < K_{e-crit} = \frac{1}{2(M+\sin(\omega t))^2} \tag{1}$$

where K_e is a dimensionless conduction parameter and is given by:

$$K_e = \frac{2L_e}{R_L T_s} \tag{2}$$

The values of the parasitic components are designed such that they follow the DCM condition such that $K_e < K_{e-crit\_min}$ and those maximum and minimum values of K_{e-crit} are as below:

$$K_{e-crit\_min} = \frac{1}{2(M+1)^2} \text{ and } K_{e-crit\_min} \frac{1}{2M^2} \tag{3}$$

Let input voltage $V_{ac=}$ 100 V_{rms} and V_o=48V power P=150W the output current is given by:

P=V×I; 150=48×I; output current I=3.125A

The output load resistance value is given by:

V_o =I×R; 48=3.125×R; R=15.34 Ω.

Let the switching frequency be 50 kHz and output voltage should be less than 1%.

$$\Delta i_{L1} < 10\% I_{L1} \quad \text{and} \quad \Delta v_{c1} < 5\% V_{c1} \tag{4}$$

$$\Delta I_{L1} = \frac{D.V_{in}}{F.L_1} \tag{5}$$

$$\Delta I_{L2} = \frac{(1-D)V_o}{F.L_2} \tag{6}$$

$$\Delta I_{L2} = \frac{(1-D)V_o}{F.L_2} \tag{7}$$

$$\Delta V_{c1} = \frac{D.V_d I_d}{V_o.C.F} \tag{8}$$

From the equations (6), (7), (8) the values of inductances and capacitances are given by:

$L_1 = L_2 = 1mH$
$L_{01} = L_{02} = 22\mu H$
$C_1 = C_2 = 1\mu F$
$C_{out} = 12000\mu F$

IV. MODELLING OF THE PROPOSED DRIVE

The bridgeless Cuk converter and PMBLDC motor are the main components of the proposed system as shown Fig 2. They are designed and modeled to form the complete drive system

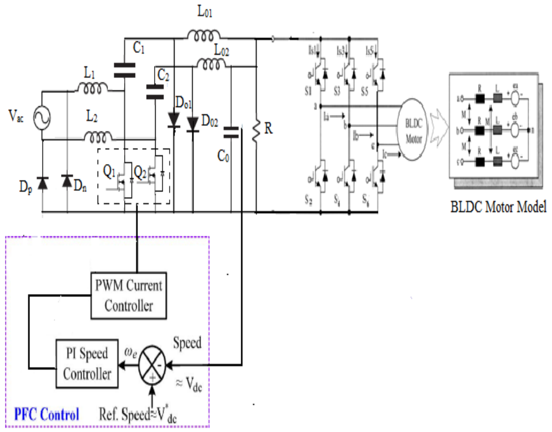

Fig 2: Proposed Drive

A. *Bridgeless PFC Converter*

The bridgeless a Cuk converter is designed as in then above section along with a speed control and PWM control.

1) Speed Controller: V_{DCref} is the reference voltage and V_{DC} is the sensed voltage at the Dc link the error voltage is given by:

$$V_{DCerror} = V_{DCref} - V_{DC} \tag{9}$$

This error signal is used to generate the pwm pulses by comparing it with sawtooth waveform.

2) *PWM controller*: The voltage error signal is compared with the sawtooth waveform and the pulses so generate will feed the switches. That is the voltage error is amplified by gain K_d and compared with fixed frequency (f_s) sawtooth waveform $S_d(t)$ to get the switching signal for the MOSFET of the bridgeless Cuk converter as

$$\text{If } K_d V_{DCerror} > S_d(t) \text{ then } S = 1 \text{ else } S = 0 \tag{10}$$

where S denotes the switching of the MOSFET of the bridgeless Cuk converter and its values “1” and “0” represent “on” and “off” conditions, respectively.

B. *PMBLDC motor drive*

The drive consists of a voltage source inverter, an electronic commutator for controlling the voltage source inverter, and the PMBLC motor.

1) *Electronic Commutator*: The electronic commutator is used to generate the switching pulses for the voltage source inverter. The rotor positions are sensed by Hall Effect sensors and emf signals are generated. This is decoded to get the respective switching signals as shown in Table 1. [2]

TABLE I
SWITCHING SIGNAL GENERATION BASED ON HALL EFFECT SENSOR SIGNALS [2]

Hall signals			Switching Signals					
H_a	H_b	H_c	S_1	S_2`	S_3	S_4	S_5	S_6
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	1	0
0	1	0	0	1	1	0	0	0
0	1	1	0	1	0	0	1	0
1	0	0	1	0	0	0	0	1
1	0	1	1	0	0	1	0	0
1	1	0	0	0	1	0	0	1
1	1	1	0	0	0	0	0	0

1) *Voltage source inverter*: The inverter just performs the conversion of DC-AC and the output of the VSI is fed to the phases of PMBLDC motor. The equivalent circuit of the VSI fed BLDC motor is shown as in Fig 3. The output of the VSI is as below:

$$V_{ao} = V_{dc}/2 \text{ for } S_1=1 \tag{11}$$

$$V_{ao} = -V_{dc}/2 \text{ for } S_2=1 \tag{12}$$

$$V_{ao} = V_{dc}/2 \text{ for } S_1=1 \text{ and } S_2=0 \tag{13}$$

$$V_{an} = V_{ao} - V_{no} \tag{14}$$

Where V_{ao}, V_{bo}, V_{co} represents the voltages between the three phases(a, b, c) and the midpoint of the DC link voltage “o” as shown in the figure. V_{an}, V_{bn}, V_{cn} are the voltages between the three phases and the neutral point "n". V_{dc} is the DC link voltage. The 1and 0 of switches S_1/ S_2 represents the on and off of the respective IGBTs. Similarly all other phases are being switched.

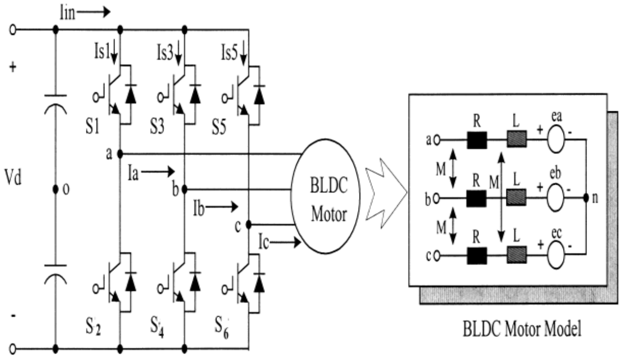

Fig 3: Equivalent circuit of VSI fed PMBLDCMD

1) *PMBLDC motor*: The PMBLDC motor can be modelled by some set of differential equations. Where different equations are used to generate speed, stator currents and back EMFs.

The PMBLDCM has three stator windings and a permanent magnet at the rotor. So the circuit equations of the phase windings are given by:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} L-M & 0 & 0 \\ o & L-M & 0 \\ 0 & 0 & L-M \end{bmatrix}$$

$$P\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \tag{15}$$

Where V_a, V_b, V_c are the phase voltages, i_a, i_b, i_c are the phase currents, e_a, e_b, e_c are the back EMFs. The dynamic equations of the phase voltage with the condition M=0 can be written as:

$$V_a = Ri_a + L\frac{d}{dt}(i_a) + e_a \tag{16}$$

$$V_b = Ri_b + L\frac{d}{dt}(i_b) + e_b \tag{17}$$

$$V_c = Ri_c + L\frac{d}{dt}(i_c) + e_c \tag{18}$$

Where R is the resistance per phase, L is the inductance. From the above stator phase currents can be generated. The electromagnetic torque is given by:

$$T_e = \sum_k K_t i_k f_k(\theta_r) \tag{19}$$

$$T_e - T_l = J\frac{d\omega_m}{dt} + B\omega_m \tag{20}$$

Where k= a, b, c. i_k is the phase current of k^{th} phase, ω_m is the rotor speed, $f_k(\Theta_r)$ is the back emf constant, T_l is load torque, J, B are the rotor inertia and damping constant respectively, and K_t is the torque constant. From (20) we can easily generate the speed.

The EMFs e_a, e_b, e_c are trapezoidal and given by the dynamic equation:

$$E_k = \sum_k K_e \omega_m f_k(\theta_r) \tag{21}$$

where K_e is the back emf constant. Electrical rotor speed and position are related by the equation

$$\frac{d\theta_r}{dt} = \frac{P}{2}\omega_m \tag{22}$$

V. PERFORMANCE EVALUATION OF THE PROPOSED DRIVE

The proposed PMBLDCM drive system is evaluated and tested in a MATLAB Simulink environment. The results are then compared with the conventional system. That is the Bridgeless Cuk rectifier fed PMBLDCM drive is compared with the conventional Cuk PFC converter fed PMBLDCM drive. They are compared in terms of efficiency, power factor etc. The simulation of the proposed system is given in Fig (4). The conventional simulation scheme is in Fig (6).

TABLE II
SIMULATION DETAILS OF THE BRIDGELESS CUK CONVERTER

Input voltage	180
Switching Frequency	10 kHz
Input inductors L_1 and L_2	1mH
Output inductors L_{o1} and L_{o2}	22μH
Energy transfer capacitors C_1 and C_2	1μF
Filter capacitors C_o	12000 μF
Active Switches Q_1 and Q_2	R_{dson}=29mΩ
Output diodes D_o, D_{o1} and D_{o2}	V_f =0.9V
Input diodes D_p and D_n	V_f =0.7V
Filter L & C	L=$1e^{-4}$ & C=$39e^{-2}$

TABLE III
MOTOR SPECIFICATIONS

Armature inductance[L]	0.0085H
Armature resistance[R]	2.8750ohm
Rotor inertia[J]	0.8e-3kg-m^2
Damping constant[B]	1e-3 N.m.s/rad
Back EMF Constant[Ke]	0.175 V.sec
Torque Constant[Kt]	1.4 N.m/A

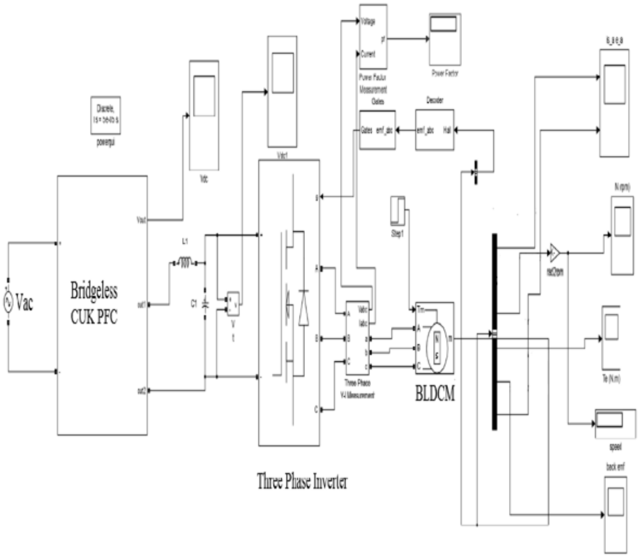

Fig 4: Simulation diagram of the proposed drive

The proposed PMBLDCM drive system’s speed, stator current, electromagnetic torque and back EMFs waveforms are as below:

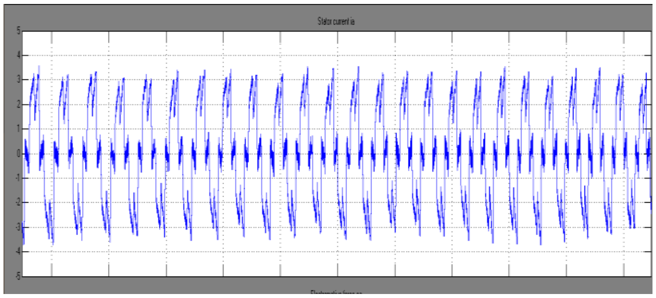

Fig 5(a)

Fig 5(a) shows the stator phase currents of one phase. Each phase currents will be 120 degree shifted. The rotor steady state speed is as in Fig 5(b) where at starting speed various and by the controller action it is set a steady state speed

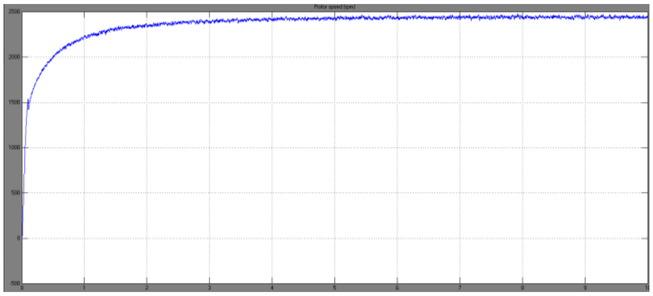

Fig 5 (b)

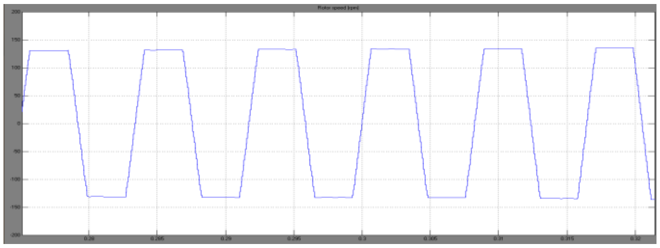

Fig 5 (c)

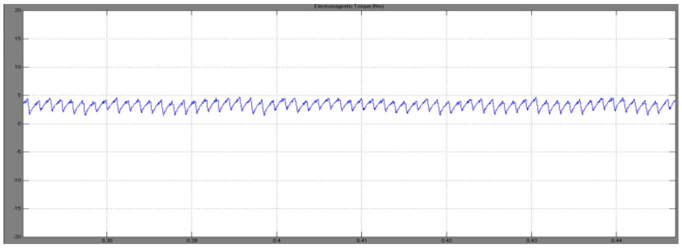

Fig 5 (d)

. The Fig 5(c) shows the quasi trapezoidal waveform. The quasi waveforms which synchronize with the trapezoidal back EMF generate a constant torque as in Fig 5(d).

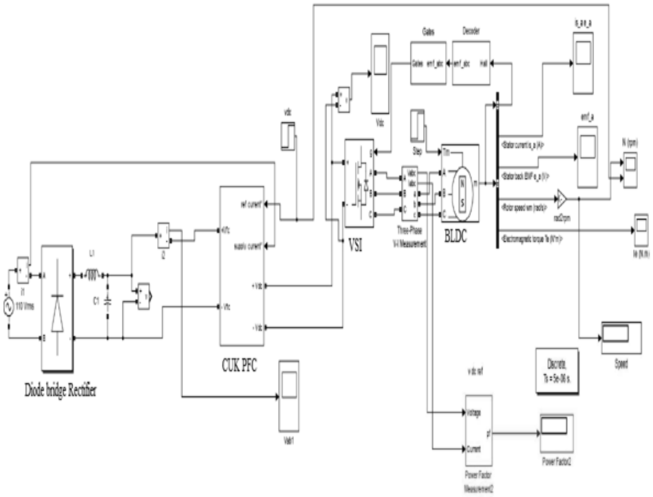

Fig 6: Simulation diagram of the Conventional Drive

The proposed drive system is then compared with the conventional Cuk PFC converter based PMBLDCM drive in terms of THD to establish that the proposed drive is efficient over the conventional system.

The THD analysis is taken for speed, back EMF, stator current and electromagnetic torque of both proposed and conventional system. Along with this the primary aim power factor correction is also checked for both of the systems and tabulated as in Table IV.

TABLE IV
PERFORMANCE DETAILS

Type	Conventional Drive	Proposed Drive
THD--Speed	133.36	65.98
THD--Back EMF	149.35	65.98
THD--Stator Current	136.92	49.35
THD--Torque	158.56	46.67
Power Factor (%)	0.997	0.993

The Table IV clearly yields the result that the proposed bridgeless Cuk converter drive has less THD as compared with the conventional drive. The less THD shows that t the proposed drive has more accurate output than the conventional drive. That is the proposed drive system is efficient over the conventional system. More over the input power factor of the same is almost unity.

VI. CONCLUSION

A new efficient permanent magnet brushless DC motor drive has been simulated and experimentally validated, so can be used with any load to yield a good efficient working system. Initially various topologies of power factor correction circuits are evaluated and the result are confined such that the best suitable one is selected. It is analyzed that a cuk converter has the best result but the problem with all the topologies is the conduction losses. So a bridgeless Cuk PFC converter is used. This converter is analyzed with the PMBLDC motor drive and the drive has unity input power factor and less conduction losses. So all together it is an efficient drive. The proposed PMBLDCMD is promising variable speed drive for air conditioning system, electric traction etc. All the problems of poor power factor, heavy inrush current, etc of can be mitigated by the proposed bridgeless Cuk PFC based PMBLDCMD.

REFERENCES

[1] J. F. Gieras and M. Wing, Permanent Magnet Motor Technology,design and Application. New York: Marcel Dekker, 2002
[2] N. Mohan, M. Undeland, and W. P. Robbins, Power Electronics: Converters, Applications and Design. Hoboken, NJ: Wiley, 1995
[3] Huai Wei, “Comparison of basic converter topologies for power factr correction” University of central Florida, Orlando, 1998.
[4] W. Choi, J.Kwon, E. Kim, J. Lee, and B.Kwon, “Bridgeless boost rectifier with lowconduction losses and reduced diode reverse-recovery problems” IEEE Trans. Ind. Electron., vol. 54, no. 2, pp. 769–780, Apr. 2007
[5] W. Wei, L. Hongpeng, J. Shigong, and X. Dianguo, “A novel bridgelessbuck-boost PFC converter,” in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 1304–1308.
[6] Yungtaek Jang, Milan M Jovanovic “Bridgeless High power factor Buck converter”, *IEEE Trans. Power Electron*., vol. 26, no. 2, pp. 291–297, Feb. 2011
[7] M. Mahdavi and H. Farzanehfard, “Bridgeless SEPIC PFC rectifier withreduced components and conduction losses,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4153–4160, Sep. 2011.
[8] Sebastian, J., Cobos, J.A., Lopera, J.M., and Uceda, J.: ‘The determination of boundaries between continuous and discontinuous conduction mode in PWM DC-to-DC converters used as power factor preregulators’, IEEE Trans. Power Electron., 1995, 10, (5)
[9] CnndA. Sabzali, E. H. Ismail, M. Al-Saffar, and A. Fardoun, “New bridgelessDCM sepic and Cuk PFC rectifiers with low conduction and switchinglosses,” IEEE Trans. Ind. Appl., vol. 47, no. 2, pp. 873–881, Mar./Apr. 2011.
[10] E. H. Ismail, Abbas.A.Fardoun, Ahmad.J.sabazali, Mustafa.A.Al-Saffar “New efficient Bridgeless Cuk rectifiers For PFC applications,” *IEEE Trans. power. Electron.*, vol. 27, no. 7, July. 2012.

BIOGRAPHY

Jomy Joy was born in Kerala, India in 1990. He obtained his bachelor degree from Anna University, Chennai. He is currently pursuing his Masters degree in Power electronics from Cochin University of science and technology, Kerala. His area of interest includes power electronics, electrical drives and electrical machines.